



INTERNATIONAL
TECHNOLOGY ROADMAP
FOR
SEMICONDUCTORS 2.0

2015 EDITION

HETEROGENEOUS INTEGRATION

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Table of Contents

1. Introduction.....	4
2. Scope	4
Mission Statement	6
3. Difficult Challenges	6
4. Single and Multi- Chip Packaging Overall Requirements	8
Electrical Requirements.....	8
Interconnect.....	9
Cross Talk.....	9
Power Integrity.....	10
Thermal Requirements	10
Single Chip Package Thermal Management.....	10
Hot Spots	12
Mechanical Requirements	13
Mechanical Modeling and Simulation.....	13
Cost	13
Reliability	13
Chip to Package Substrate.....	13
Interconnect Technologies for Single Chip Package.....	14
Wire Bonding	14
Package Substrate to Board Interconnect.....	15
For Low-Cost Applications—Laminate for PBGA (Table HI-6)	15
Mobile Applications—Build-up Substrate for SiP (HI-7).....	15
Cost Performance Applications—Build-up Substrate for FCBGA (table HI-8).....	15
High Performance—Low κ Dielectric Substrate for FCBGA (Table HI-9).....	15
High Performance (LTCC) (table HI-10).....	15
5. Wafer Level Packaging.....	16
Overview	16
Embedded Wafer Level Packaging	19
Wafer Level Package Developments and Trends	22
Future Trends for Wafer Level Packaging	23
Examples for Emerging Wafer Level Package Technologies.....	24
Fan Out WLP Using Reconfigured Wafer Level Technologies	24
Difficult Challenges for WLP	25
6. 2.5 D Integration	26
7. 3D integration	27
Difficult Challenges for 3D integration	29
3D Integration Definition of Terms.....	29
Processes for 3D-TSV integration	30
Technology Requirements.....	31
TSV Formation	31
TSV Interconnect Methods.....	32

Wafer/Device Stacking	32
Micro Bump Formation Process	35
Requirements for high k dielectrics with high breakdown field	36
3D Issues.....	36
Heterogeneous 3D stacking process	37
Emerging inter-die interconnect and bonding technology	38
3D Integration of Logic and Memory	40
Power Integrity.....	41
Thermal Management	41
Test for 3D Integration.....	44
Reliability in 3D Integration.....	44
8. System Level Integration in Package (SiP)	45
SiP versus SoC	46
Definition of SiP	46
SiP Implementations and Package on Package	47
Package-on-Package (PoP).....	50
Future Complex 3D SiP	51
SiP-Level System Design versus Board-Level System Design.....	52
Difficult Challenges for SiP	53
Thermal Management for SiP.....	53
Thermal Challenge of Hot Spots in SiP.....	53
Cooling Solution Design Requirements for SiP.....	53
Thermal Challenges of Processor and Memory Die Stacked SiP.....	54
Power delivery/power integrity.....	55
Testing of SiP	55
Test access	56
Contacts	56
Mechanical and Thermal Testing	56
Cost of Test	56
Difficult Challenges for SiP	57
Power requirements and integrity.....	57
Thermal Management	58
Physical density of Bandwidth.....	58
9. The Need for Coherent chip-package-system co-design, Modeling and Simulation	58
Overall Requirements.....	59
Co-Simulation of RF, Analog/Mixed Signal, DSP, EM, and Digital	60
Collaboration, Cost and Time to Market.....	60
Design for Reliability in SiP	60
Generic Chip-Package-System Co-Design Tool Requirements	61
10. Packaging for Specialized functions.....	62
Technical Challenges	62
TSV.....	62
Advanced Packaging -- SiP and PoP.....	62
Optics	62

Electrical connectors for packages and cards.....	63
Low-loss electrical for packages and cards	63
Efficient power distribution	63
Optoelectronic Packaging.....	64
Scope	64
Photonic Sensors	65
Optical Data Transmission	66
Silicon Photonics	66
Package Test Difficult Challenges.....	68
Difficult Packaging Challenges by Circuit Fabric.....	69
Packaging for MEMS.....	70
Semiconductor Packaging for Automotive Applications	72
Automotive electronics	72
Packaging technology development.....	73
11. Advanced Packaging Processes.....	74
Scope	74
Embedded and Integrated Passive and Active Devices.....	74
Embedded passive devices	75
Embedded Active Devices	76
Wafer Thinning and Singulation	77
12. Packaging Materials Requirements.....	79
Scope	79
Dielectric Materials	82
Solid and Porous Polymers.....	82
Low κ and Ultra-low κ Dielectrics.....	82
High κ Dielectrics.....	83
Polymers	83
Die and other component Attach Materials	83
Conductors	85
Ceramics	85
Nano-materials	86
Composite materials.....	87
Barrier layers.....	87
13. Reliability.....	88
Packaging Reliability	88
Scope	88
Physics of Reliability.....	88
Component Interaction Reliability Issues.....	89
Failure Mechanisms	89
Potential Solutions.....	90
Conclusion.....	91
References	91
14. Packaging Gaps and Technology Needs	92
Acknowledgement.....	92

1. INTRODUCTION

The electronics industry is nearing the limits of traditional CMOS scaling. The continued growth of the industry, driven by a continuous reduction in cost per function, will require new device types, new package architectures and new materials. There may be a gap between the time CMOS scaling can no longer maintain progress at the Moore's Law rate and the time a new generation of device architectures and electronic material will support a continued drop in cost per function. As traditional Moore's law scaling becomes more difficult, innovation in assembly and packaging enabling functional diversification through Heterogeneous Integration (HI) and allowing scaling in the third dimension must take up the slack. The Heterogeneous Integration Focus team incorporates by reference the Test and Interconnect Technical Working Group Chapters. Assembly and Packaging provides a mechanism for cost effective incorporation of functional diversification through System-in-Package (SiP) technology. This technology enables the continued increase in functional density and decrease in cost per function required to maintain the progress in cost and performance for electronics. This will provide the principle mechanism for delivering cost effective functional diversification and thereby, equivalent scaling, to maintain the pace of progress.

New architectures including printed electronic circuits, thinned wafers and both active and passive embedded devices are emerging as solutions to market requirements. The materials and equipment used in assembly and packaging are also changing rapidly to meet the requirements of these new architectures and the changing environmental regulatory requirements.

One important requirement for scaling cost is to establish and maintain an efficient supply chain. This requires coordinating activity for multiple IDMs, Foundries, and test companies. An efficient supply chain should naturally concentrate activities to reduce cost and adopt standards to ensure competition. As innovation increases to meet market performance requirements, maintaining an efficient packaging supply chain will be a significant challenge. Products will come from multiple vendors and be delivered as packaged product to consumer electronics companies all want to differentiate their product. Improved approaches to ensure an efficient supply chain will be needed.

2. SCOPE

The Heterogeneous Integration Chapter will address the assembly & packaging, test and interconnect technologies required to meet industry needs over the next 15 years by incorporation of the Assembly and packaging TWG material and, by reference, the Test and Interconnect TWG Chapters. The incorporation of functional diversity and system level integration enabling System-in-Package architecture is the key contribution of Heterogeneous Integration.

Assembly and Packaging is the final manufacturing process transforming semiconductor devices into functional products for the end user. Packaging must provide electrical and photonic connections for signal input and output, power input, and voltage control. It also provides for thermal dissipation and the physical protection required for reliability. The rise of the Internet of Things (IoT), movement to the cloud of data logic and applications,

the slowing of Moore's Law scaling for CMOS and the realization that transistors at the geometries to be used will wear out all place new demands on assembly and packaging.

The focus for Heterogeneous Integration (HI) is identification of the difficult challenges and the potential solutions for meeting those demands for the next 15 years. The primary integration technology for the potential solutions will be complex, 3D System in Package (SiP) architectures.

Today assembly and packaging is a limiting factor in both cost and performance for electronic systems. The historical failure of packaging performance and cost to scale as integrated circuits scale has resulted in packaging becoming and increasing percentage of product cost and this failure continues today. This is stimulating an acceleration of innovation. Design concepts, packaging architectures, materials, manufacturing processes and systems integration technologies are all changing rapidly. This accelerated pace of innovation has resulted in development of several new technologies as well as expansion and acceleration of technologies introduced in prior years. Heterogeneous integration with wireless and mixed signal devices, bio-chips, power devices, optoelectronics, and MEMS in a single package is placing new requirements on packaging and assembly as these diverse components are introduced as elements for System-in-Package (SiP) architectures.

There will be innovation required in single chip packaging to address new device types such as photonic components and new power devices which will require new materials, new processes and new production equipment. The single chip packaging Roadmap is in Section 4 and has 9 tables addressing the attribute requirements.

The SiP section is complex due to the large number of diverse system requirements that must be addressed. We have selected representative SiP types to bring focus to the diverse requirements and potential solutions. The Chapter takes into account requirements for:

- ✓ High performance computing
- ✓ High speed, low latency communications
- ✓ Internet of things
- ✓ Consumer products

This chapter is organized in 12 subchapters:

- Difficult Challenges
- Single Chip Packaging and Multi-chip Packaging
- Wafer Level Packaging; fan-in and fan-out
- 2.5D Integration
- 3D Integration
- System Level Integration in Package (SiP)
- The Need for Coherent chip-package-system co-design, Modeling and Simulation
- Packaging for Specialized Functions
- Advanced Packaging Processes

Packaging Materials Requirements
Reliability
Packaging Gaps and Technology Needs

Wherever possible we have aligned the ITRS Heterogeneous Integration Chapter with other industry roadmap organizations including iNEMI, JISSO, MIT's Communication Technology Roadmap and IPC.

MISSION STATEMENT

Heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics.

In this definition components should be taken to mean any unit whether individual die, MEMS device, passive component and assembled package or sub-system that are integrated into a single package. The operating characteristics should also be taken in its broadest meaning including characteristics such as system level cost of ownership.

The mission of the Heterogeneous Integration Focus Team is to provide guidance to industry, academia and government to identify key technical challenges with sufficient lead-time that they do not become roadblocks preventing the continued progress in electronics that is essential to the future growth of the industry and the realization of the promise of continued positive impact on mankind. The approach is to identify the requirements for heterogeneous integration in the electronics industry through 2030, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions.

3. DIFFICULT CHALLENGES

Several key limitations faced by the Semiconductor industry in the near term will involve most, if not all, of the Technical Working Groups (TWGs) and Focus Teams. These include:

- Manage the power and thermal dissipation requirements through both reduction in power requirements and improving the heat dissipation capability of packages.
- Increasing the physical density of bandwidth in order to make use of the enormous gains in the physical density of processor power.
- Support the growing functional diversity requirements driven by “More than Moore” technologies.
- Support the reliability, power integrity and thermal management challenges of 3D integration.
- Drive down cost in assembly and packaging to reduce the impact of packaging cost not scaling to match device cost.

- Reduce time to market and by co-design and simulation that includes electrical, thermal, mechanical and, in some cases chemical, requirements for the device, package and system.
- Support reliability in the face of transistors that will wear out.
- Support the global network changes required to handle the coming yottabyte (10^{24}) level data traffic requirement.
- Developing designs, equipment, materials and processes to support the introduction of 450mm wafer production.

The difficult challenges for the HI Roadmap are presented in Table HI-1. These challenges provide more specific granularity for packaging than the list above. Difficult challenges for geometries greater than 16 nm are presented in the table below. There has been a rapid pace of change in materials, processes and architectures to meet these challenges in the last few years and this progress continues. To maintain the rate of progress the difficult challenges in the table below must be overcome.

<i>Table HI-1 Heterogeneous Integration Difficult Challenges</i>	
Difficult Challenges ≥ 16 nm	Summary of Issues
Impact of BEOL including Cu/low κ on packaging	– Improved fracture toughness of dielectrics
	– Interfacial adhesion
	– Probe damage for copper/ultra low κ
Wafer level Packaging	– 3D integration in WLP
	– Embedded components in WLP
	– CTE mismatch compensation for large die and fan-out die
System in Package	– Cross talk due to increased circuit density
	– Thermal density and hot spots
	– Heterogeneous integration of different semiconductor materials
	– Heterogeneous integration of different circuit types (logic, memory, analog, RF, MEMS, power, passives etc.)
Coordinated design tools and simulators to address chip, package, and substrate co-design	– Mixed signal co-design and simulation at system level with heterogeneous integration
	– Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis
	– Electrical (signal and power integrity with higher frequency/current and lower voltage operation)
	– Models for reliability prediction
Interposers and Embedded components	– CTE mismatch and warpage for large interposers
	– Embedded active devices
	– Electrical and optical interface integration, thermal interface
Thinned die packaging	– Handling technologies for thinned die and wafers (particularly for bumped wafers)
	– Testability

The challenges for geometries below 16 nm include the items listed below. These challenges reflect the fundamental changes associated with continued scaling. The challenges are complex and will require substantial innovation.

<i>Difficult Challenges ≤16 nm</i>	<i>Summary of Issues</i>
Close gap between chip and substrate, Improved Organic substrates	-Increased wireability at low cost
	-Improved impedance control and lower dielectric loss to support higher frequency applications
	-Silicon I/O density increasing faster than the package substrate technology
3D assembly and packaging	-Thermal management
	-Alignment/placement accuracy layer to layer
	- Test access for individual wafer/die
	-Cost of TSV and cost of Interposer
	-Bumpless interconnect architecture
Package cost does not follow the die cost reduction curve	- Wafer level packaging and 3D equipment cost is not scaling with product (transistor) cost
	- Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	- Electromigration at high current density for interconnect (die, package).
	- Thermal dissipation
	- Improved current density capabilities
High frequency die	- Lower loss dielectrics
	- “Hot spot” thermal management
Power Integrity	- Power delivery in stacked die
	- Reducing power supply voltage with high device switching currents

4. SINGLE AND MULTI- CHIP PACKAGING OVERALL REQUIREMENTS

ELECTRICAL REQUIREMENTS

Manufacturing tolerances have a major impact on the performance of electrical designs. The manufacturing tolerance roadmap reflected by the tables, for via diameter, via alignment, metal thickness; line width and dielectric thickness must be aligned with the electrical requirements. The major issues defining requirements for single chip packages are discussed below. The single chip packaging technology requirements are defined in table HI-2.

Heterogeneous integration at the package level results in new electrical challenges. The use of the third dimension adds further to the complexity of the problem. The reduction of total power requires operation at the lowest possible voltage at the highest reliable frequency. The result is a need for decoupling inductance with capacitors located at the transistors to maintain voltage independent of the operation being performed and reduced

ground resistance. It also requires shielding within the package to isolate RF and digital signals and the associated antenna structures. This will present increasing challenges as voltages are reduced, transistor count is increased, HI incorporates components with different power and thermal requirements and analog, mixed signal, power management, RF and photonics into the same package.

INTERCONNECT

On package interconnect is limited to electrical signals and that is addressed in this section. The introduction of on-package photonic interconnect will be addressed in section 9 under Optoelectronic Packaging for data transmission. The electrical interconnect has several difficult challenges related to cross talk, power integrity, thermal management and electromigration. These issues increase in severity as the cross section of the conducting wires decreases, diverse elements come closer together and the operating voltage is decreased. It is well known that:

- Copper increases in resistivity at very small geometries due to increased edge and grain boundary scattering
- Inductance increases as wire cross section is decreased and complex geometries are used

These issues increase latency for data signals and threaten power integrity, particularly for 3D integration. Improvements can be made in design but these alone will not be sufficient to meet requirements over the life of this roadmap. Potential solutions will require incorporation of passive devices into the interconnect and new materials to satisfy the materials properties requirements. For example we will need:

- Conductors with higher conductivity and reduced electromigration
- Dielectrics with a lower κ to reduce interconnect capacitance
- Higher κ dielectrics with low leakage and high breakdown field strength to decouple inductance close to the transistors

The requirements for new materials are described in more detail in section 12 of this chapter.

CROSS TALK

The shrinking of die and package dimensions and the incorporation of diverse circuit fabric types through heterogeneous integration increases the challenges of controlling cross talk between circuit elements. There are potential solutions to address these challenges but, in many cases, the solution will be a combination of new design rules, new materials and the addition of new features.

The design rules are application specific. For example, long signal traces that are closely spaced in a design may experience cross talk due to the electric field interaction of data signals on adjacent traces. A solution can be design rules that for, a specified voltage specifies a minimum spacing between signal traces. This increase the package size therefore more complex design rules might require a ground trace between signal lines.

The design tools today are adequate to address this issue but as packages continue to shrink this will be an increasing problem.

The incorporation of RF components, including antenna structures, cannot be handled by spacing design rules. In this case the package design must incorporate a shield between RF components and any other component that can radiate energy inside the package such as very high speed switching of transistors.

New materials that enable high Q factor passive components of very small size will allow incorporation of local filters into the package and die interconnect to reduce cross talk noise. Higher conductivity conductors, lower κ dielectrics to reduce interconnect capacitance, higher κ dielectrics to enable small area capacitors to decouple inductive switching energy and improved inductors will all be needed to meet future requirements.

POWER INTEGRITY

The decrease in operating voltage to less than 400mv to reduce power demand requires that we maintain the accuracy of the voltage of the transistors with respect to package ground at +/- 40mv or better. This is a more difficult challenge for 3D integration and will be address in the 3D integrations portion of section 8 of this chapter.

THERMAL REQUIREMENTS

Temperature control is critical for the both operating performance and long term reliability of single chip and SiP packages. The high junction-to-ambient thermal resistance resulting from a thermal management device such as a heat sink provides inadequate heat removal capability at the necessary junction temperatures for ITRS projections at the end of this roadmap. Today, a massive heat sink, which may be larger than the chip by orders of magnitude, is attached to a silicon chip through a potential presence of a heat spreader and variety of thermal interface materials (TIM). Not only does this insert a large thermal resistance between the chip and the ambient, it also limits the chip packing density in electronic products thereby increasing wiring length, which contributes to higher interconnect latency, higher power dissipation, lower bandwidth, and higher interconnect losses. The ITRS projected power density and junction-to-ambient thermal resistance for high-performance chips at the 14 nm generation are $>100 \text{ W/cm}^2$ (however from a localized point of view, it can be $> 4\sim 5 \text{ uW/um}^2$) and $<0.2^\circ\text{C/W}$, respectively. The main bottlenecks in reducing the junction-to-ambient thermal resistance are the thermal resistances of the thermal interface material (TIM), all interfaces in the path and the heat sink itself.

SINGLE CHIP PACKAGE THERMAL MANAGEMENT

New passive and forced liquid and phase change (liquid to gas) active heat sinks are in limited use today and are addressed in more detail in the System in Package section of this chapter. They hold the promise of decreased thermal resistance and improved heat spreading capability to address the effect of hot spots.

Field Programmable Gates Arrays (FPGAs) serve a wide range of applications with diverse thermal and packaging requirements. There are two mainstream packages for today's FPGA solutions: wire bond BGA (WBBGA) and flip chip BGA (FCBGA). The WBBGA package has a lower thermal performance, with devices dissipation 5-10W, and they are used in low-end applications. The FCBGA package has a higher thermal performance, with devices dissipating 10-150W, and they are used in mid-range and high-performance applications.

There are two parts to the equation of thermal management: package and system components. Typically, component suppliers control the package part and customers or system integrators control the system part. The system part typically has larger thermal resistance than the package part and cooling solutions are generally required to reduce it. In today's rack and blade type networking solutions, typical applications of high-end FPGAs, the heat sink design needs to accommodate all the devices in the system. The typical ambient temperature can vary from -40 to +60C depending on system-level cooling solutions. One of most thermally demanding applications of a mid-range FPGA is Remote Radio Head (RRH) in cell phone towers, where high system performance is required but there is no active cooling and air flow. In addition, the device operates in thermally extreme environmental conditions where the ambient temperature can vary from 50-60C.

In both mid-range and high-end FPGAs, the total power dissipation is already stretching the envelope of traditional cooling solution. The FPGA vendors are expected by their customers to improve system performance by 2X every generation within same power budget (i.e. 2X improvement in Performance/watt). Traditional process scaling provides only ~20-30% improvement in Performance/Watt. To bridge this performance-power gap, innovations in FPGA and system architecture, power management, and cooling solutions are required. Future systems will deploy high-bandwidth multi-die technologies such as silicon interposer based 2.5D and vertical stacking based 3D integration to improve system capabilities and offer differentiated products. Thermal challenges will likely exacerbate FPGA based 3D integration unless innovative cooling solutions are available. (See Section 6 of this Chapter)

To improve thermal performance of WBBGA package in next 1-2 process nodes, it is desirable to increase thermal conductivity of epoxy mold compounds (EMC) by 2-3X through material innovation. In addition, structural innovation to traditional WBBGA package to improve thermal performance may be required. For FCBGA packages, the primary heat removal path is through the case of the package and optimizing junction-to-case thermal resistance is the most important thermal parameter for FCBGA packages. Reduction in bond line thickness (BLT) and use of high thermally conductivity thermal interface material (TIM) to reduce junction-to-case thermal resistance by more than 50% will be required in future systems. In addition to addressing thermal performance, these solutions have to be cost-competitive, manufacturable, and reliable. Typically, FPGAs are deployed in systems for 10-15 years and long-term sourcing and reliability are among some of the key requirements.

HOT SPOTS

Hot spots refer to local areas in the chip, typically of the size of tens to hundreds micrometers, which yield local heat fluxes in excess of several multiples of the background (or average) heat fluxes over the entire area of the chip. While the total power generated at the hot spot is typically very small, of the order of few Watts or even sub-Watt, the small footprint area over which this power is released presents a daunting challenge to the existing heat removal methods and cooling technologies. The last consideration that is uniformly applicable to all possible hot spot cooling methods, regardless of their physical principle, is that it has to be brought within a distance of the size of the hot spot itself in order to have any cooling effect, and this challenges at the very core the existing manufacturing and packaging techniques that implement the cooling approach/technology as part of the chip and package. Some recent examples on cooling of hot spots in microprocessors using three fundamentally different technologies are:

1. Evaporative liquid cooling within nanoscale confined domains focusing on achieving the highest possible heat flux dissipation
2. Hybrid solid state-microfluidic cooling aiming to synergistically cool both the hot spots, on-demand with fast transient response, and background power load
3. Embedded solid-to-liquid phase change “thermal capacitors” to achieve fully passive cooling of buried hot spots with dynamically variable duty cycles.

This discussion is not intended to provide the comprehensive coverage of existing work in this area. Solutions proposed include use of carbon nanotubes, micro-refrigerators, heat pipes, thermoelectric and an interested reader is referred to the few papers we cite, which include comprehensive reviews of the state of the art in their respective technology domains.

Applied Energy, [Volume 138](#), 15 January 2015, Pages 414–422

Energy efficient hotspot-targeted embedded liquid cooling of electronics

[Chander Shekhar Sharma^a](#), [Manish K. Tiwari^{a,1}](#), [Severin Zimmermann^a](#), [Thomas Brunswiler^b](#), [Gerd Schlottig^b](#), [Bruno Michel^b](#), [Dimos Poulikakos](#)

Applied Thermal Engineering, [Volume 64, Issues 1–2](#), March 2014, Pages 76–82

Water cooled minichannel heat sinks for microprocessor cooling: Effect of fin spacing;

[Saad Ayub Jajja^{a,*,1}](#), [Wajahat Ali^a](#), [Hafiz Muhammad Ali^a](#), [Aysha Maryam Ali^b](#)

Microelectronics Reliability, [Volume 52, Issue 11](#), November 2012, Pages 2660–2669

Effects of TSVs (through-silicon vias) on thermal performances of 3D IC integration system-in-package (SiP)

[John H. Lau^{a,*,1}](#), [Tang Gong Yue^b](#)

MECHANICAL REQUIREMENTS

MECHANICAL MODELING AND SIMULATION

The short design cycle and the increasing demand for customization at the system level in today's consumer dominated markets do not allow for fabricating prototypes, testing, design revisions, refabricating and retesting until this design optimization produces a product meeting all requirements including reliability. The only solution is to perform the design optimization in the computer. This requires a full suite of co-design tools and simulation capability at the system level. It must also include detailed thermal, mechanical and electrical properties of each material/component in the system. Today the thin layers of dissimilar materials incorporate into SiP products do not exhibit bulk properties. The properties are dominated by the interfaces between layers. These interface dominated materials properties are not characterized today and this will become a critical need as the layers of dissimilar materials continue to decrease in thickness. There has been much progress recently but the tools available today do not provide the full solution that is needed.

Warpage due to processing temperatures well above use case temperatures is an increasing problem as layers are thinner and package area is larger. The issue of package warpage at peak processing temperature is addressed in table HI-3. The ultimate solution for this problem is to reduce CTE mismatch with new materials and reduce induced stress by reducing processing temperature and therefore the gap between processing temperatures and use case temperatures.

COST

Focus should be on the cost drivers in the future and potential solutions to reduce cost. Address the issues limiting scaling of packaging cost as cost of die scales. Can we replace cost per pin with some other data. Addressing Materials, equipment, test and yield as major cost drivers? We will use this approach as part of addressing the cost issue. Identify the major components of cost to focus the resources on the limits. Use specific devices to address in detail (WLCSP, QFN). **This approach needs to be used to identify the cost elements of TSV for 3D integration.**

RELIABILITY

The package failure modes are presented in table HI-11. The major categories are crack formation, interfacial delamination, and void or pore formation and material decomposition.

CHIP TO PACKAGE SUBSTRATE

There are several factors that drive the selection of the appropriate chip to package substrate technology. The issues are addressed in Table HI-4: Chip-to-Package Substrate Technology and Table HI-5: Substrate to Board Pitch. The specific technologies are discussed in the sections below.

INTERCONNECT TECHNOLOGIES FOR SINGLE CHIP PACKAGE

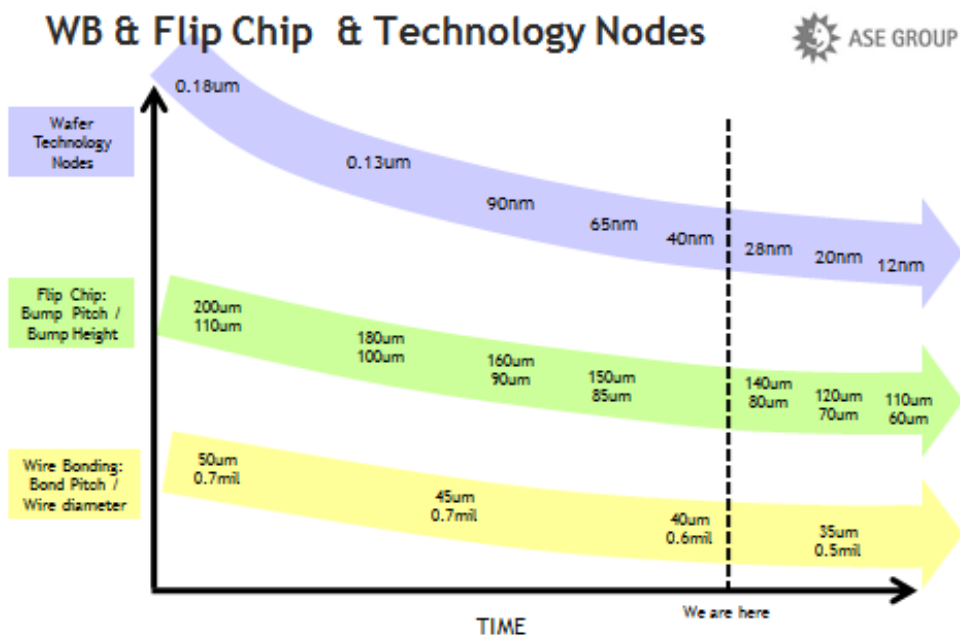
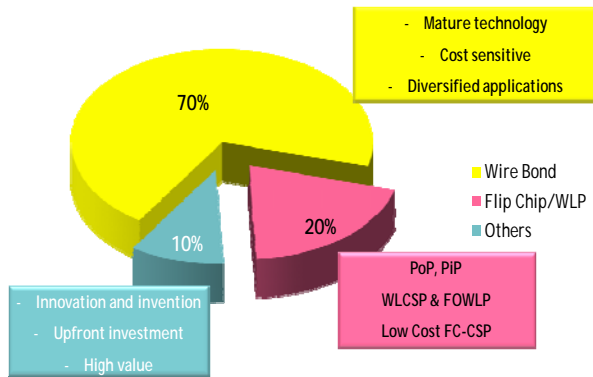


Figure 1: Wirebond and Flip Chip Pitch vs. technology nodes

WIRE BONDING

Wire bonding has been the workhorse of the semiconductor industry. It is the dominant method for interconnects for semiconductor device assembly and packaging. IC devices, wire bonded to various forms of lead frames and organic substrates and molded in epoxy molding compounds, have been the standard of the industry for years. Despite repeated

predictions that wire bond technology has reached its practical physical limit, wire bond technology continues to re-invent itself with new innovative concepts and technology improvements. Today it has been estimated that 70% or more of the world semiconductor components are packaged in wirebond.

PACKAGE SUBSTRATE TO BOARD INTERCONNECT

PACKAGE SUBSTRATES

IC substrates serve as the connection between IC chip(s) and the PCB through a conductive network of traces and holes. IC substrates support critical functions including circuit support and protection, heat dissipation, and signal and power distribution.

IC substrates represent the highest level of miniaturization in PCB manufacturing and shares many similarities with semiconductor manufacturing.

Several solutions are available depending upon a specific application. See tables for additional information.

For Low-Cost Applications—Laminate for PBGA (Table HI-6)

Mobile Applications—Build-up Substrate for SiP (HI-7)

Cost Performance Applications—Build-up Substrate for FCBGA (table HI-8)

High Performance—Low κ Dielectric Substrate for FCBGA (Table HI-9)

High Performance (LTCC) (table HI-10)

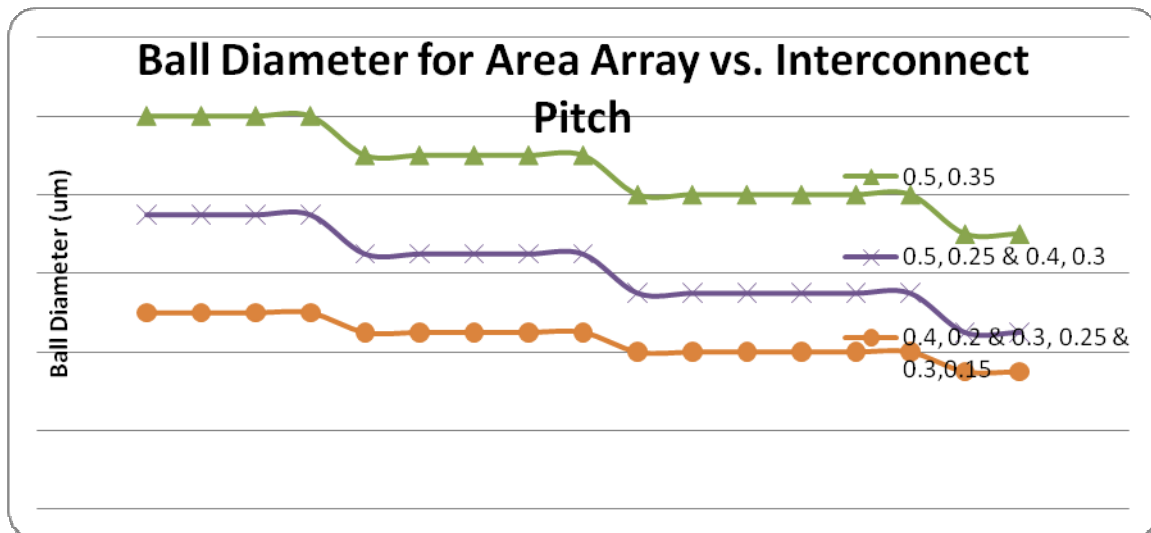


Figure 2: Ball Diameter vs. Pitch for Area Array Interconnect

5. WAFER LEVEL PACKAGING

OVERVIEW

Wafer Level Packaging (WLP) has been defined as a technology in which all of the IC packaging process steps are performed at the wafer level. The original WLP definition required that all package IO terminals be continuously located within the chip outline (fan-in design) producing a true chip size package. This definition described a Wafer Level Chip Scale Package, or WLCSP, with the processing of a complete silicon wafer. From a systems perspective, under this definition, the limitation on WLP was how many I/O could be placed under the chip and still have a board design that can be routed. WLP can provide a solution when requirements for a continued decrease in size, increase in IC operating frequency and demand for cost reduction are not met by traditional packaging e.g. wire bonding or flip chip bonding.

However, there are products coming to market that do not fall under this earlier definition of WLP. These new packages have been described as “Fan-out” WLP. They are constructed by placing individual sawn die into a polymer matrix or silicon carrier that has the same form factor as the original silicon wafer. These “Reconstituted” artificial wafers are then processed through all of the same processes that are used for “real” silicon wafers, and finally sawn into separate packages. The dice are spaced in the polymer matrix such that there is a perimeter of polymer surrounding each placed die. This can be used during redistribution (RDL) to “fan out” the RDL to an area larger than the original die. Embedded Wafer Level Packaging (eWLP) is a modification in which a reconstituted artificial molded wafer is fabricated with subsequent application of thin film technology. The main driving force behind the eWLP technology allows better fan-out and more space for interconnect routing.

This allows a standard WLP solder ball pitch to be used for die that are too small in area to allow this I/O pattern without “growing” the die to a larger size. With the implementation of this technology, it is no longer only intact silicon wafers that can be processed as a “WLP”, but hybrid silicon/polymer matrices in wafer form that also can be now classified as WLP products.

WLP technology includes wafer level chip size packages (WLCSP), Fan-out wafer level packages, wafer capping and thin film capping on a MEMS, wafer level packages with Through Silicon Vias (TSVs), wafer level packages with Integrated Passive Devices (IPD), and wafer level substrates featuring fine traces and embedded integrated passives. There are wafer-to-wafer stacking technologies that will support stacked die WLP for future products to reduce cost. While many of these technologies are still in the developmental stage they represent solutions to cost, power level reduction, performance and size challenges for consumer products in the future.

Wafer Level CSP was the first generation of a wafer level package product to be introduced into the market place. Today WLP technology (fan-in WLP) with and without redistribution layers (RDL) is used for a large variety of products. WLPs with fan-in design today are typically for low I/O count and small die sizes, although the I/O count

for today's products exceed 150. They are mainly being used in portable consumer markets where small size, thickness, weight, and electrical performance are additional advantages to cost. Major trends include work for cost efficient rerouting with multi-layer RDL and improved design and simulation tools for WLP technologies. According to JEDEC fan-out WLP can be considered as Ball Grid Array type packages. In these packages, front-end wafer technology and packaging technology merge. Panel processing can also be applied as a variation of fan-out WLP and, in this case, silicon/packaging technologies merge with printed circuit board technologies to increase parallelism in production and further reduce cost.

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With the introduction of TSVs, IPDs, Fan-out, and MEMS packaging technologies, WLP products can be used in a much broader range of applications, with higher I/O counts, and greater functional complexity. These packaging technologies open new opportunities for WLPs in the packaging field.

WLP now incorporates many different structures to meet specific application targets. A variety of WLP types are shown in Figure 3 below. Table HI-12 presents the technology requirements.

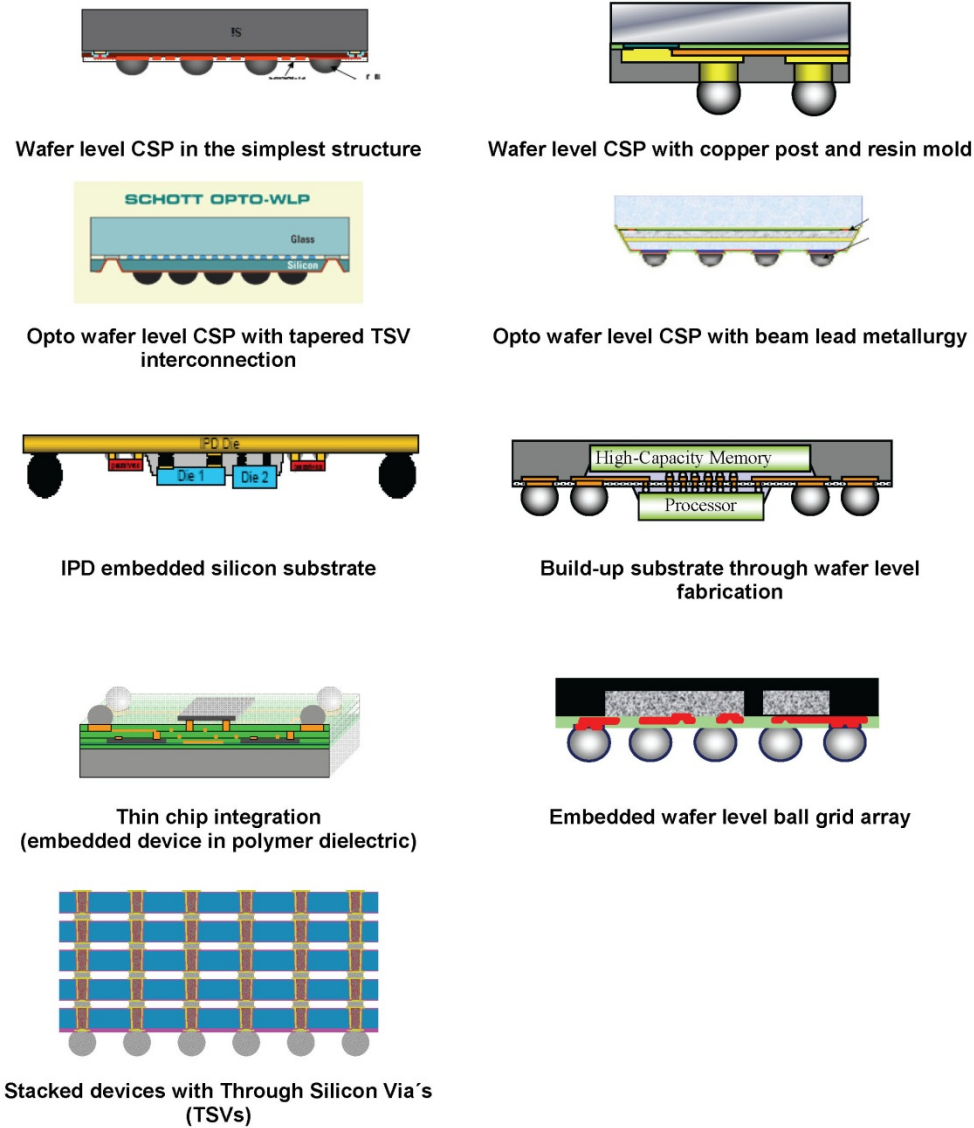


Figure 3 Examples of existing Wafer Level Packaging Types

The manufacturing process technology and high volume infrastructure enabling wide spread implementation of Wafer Level CSP in the market place have been based upon the adoption and implementation of established flip chip wafer bumping (under bump metallurgy, solder bumping, repassivation, redistribution, wafer inspection, wafer probing) processes and equipment in the merchant market. The infrastructure has been developed to serve the high volume needs of flip chip packaging in the high performance and cost performance markets. The many different WLP structures available today ranging from a simple structure like WLCSP with copper post and resin mold which require only one sputtering process and three masks to very complex structures which require thin encapsulation, back grinding and other 3D and embedded device processes. This process complexity will increase as the industry seeks to move more processes to wafer level to reduce cost.

In contrast to flip chip assembly, WLP assembly typically does not require underfill. For solder joining, solder balls are typically used with a diameter larger than 250 μm . However, for specific applications where low package height is required, smaller solder balls can be used for lower stand-off heights. The smallest pitches used in the market are 0.35 mm and 0.2 mm is sampling. For standard WLP under-fill may be used to meet specific reliability requirements such as drop test.

The traditional drop ball WLCSP designs and processes are being further developed with modifications to the stress absorbing layers, under-fill in board level assembly, and stress absorbing bump structures to allow for larger die applications. Thicker copper trace redistribution features have been introduced for higher reliability, higher power and lower signal loss applications. These trends will continue and WLP is adopted for larger and higher power die in the future.

The processes developed for copper redistribution layers are being introduced and extended to the fabrication of copper studs and passive components such as inductors, to be followed by capacitors and resistors (see section on passive devices). The combination of these components will lead to capabilities for the fabrication of filters and other sub-system circuit elements. Integration of these components into WLP-SiP packages constitutes a next step towards 3D wafer integration. The realization of vertical interconnected devices/chips using through silicon vias is one of the key emerging trends in wafer level packaging. This technology offers significant advantages in terms of electrical performances, e.g., signal transmission, interconnect density and reduced power consumption as well as form factor, heterogeneous integration, and manufacturing cost reduction.

Memory devices are being used in portable consumer products such as cell phones and PDAs in increasing quantities. WLP offers advantages in these applications, due to inherent lower cost, improved electrical performance, and lower power requirements. Key enabling technologies to take full advantage of WLP for these applications will be the development of cost effective wafer level test and burn-in.

EMBEDDED WAFER LEVEL PACKAGING

Embedded packaging refers to a variety of concepts, intellectual property, manufacturing infrastructure and related technologies. It is possible to divide embedded packaging into two main categories. The first is based on a molded wafer structure and has its starting point as a fan-out wafer level package. The second is based on a PCB or PWB substrate technology and has its starting point as a package substrate as illustrated in Figure 4 below. In every implementation Protected Known Good Die (KGD) is a key technology for embedded component integration.

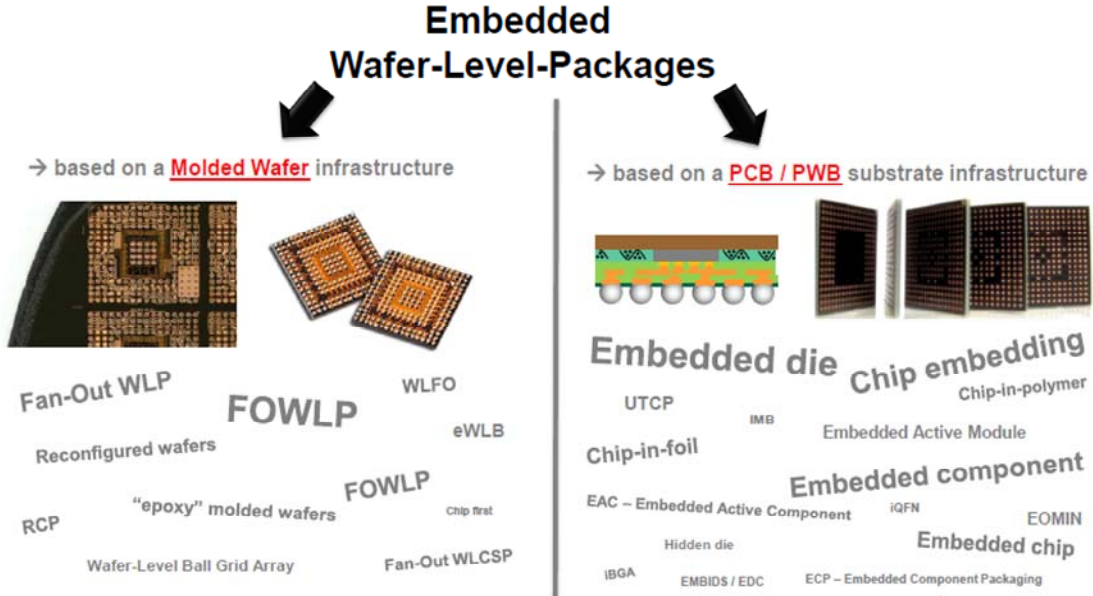


Figure 4: Molded Wafer Vs. Package Substrate embedded package base

There are now two types of embedded wafer level packages emerging one assembled entirely using a reconfigured base and the other assembled on a PCB Panel with embedded WLP components included in the assembly as illustrated in Figure 5 below.

- FOWLP is based on a **reconfigured molded wafer** infrastructure
- Embedded die is based on a **PCB type of Panel** infrastructure

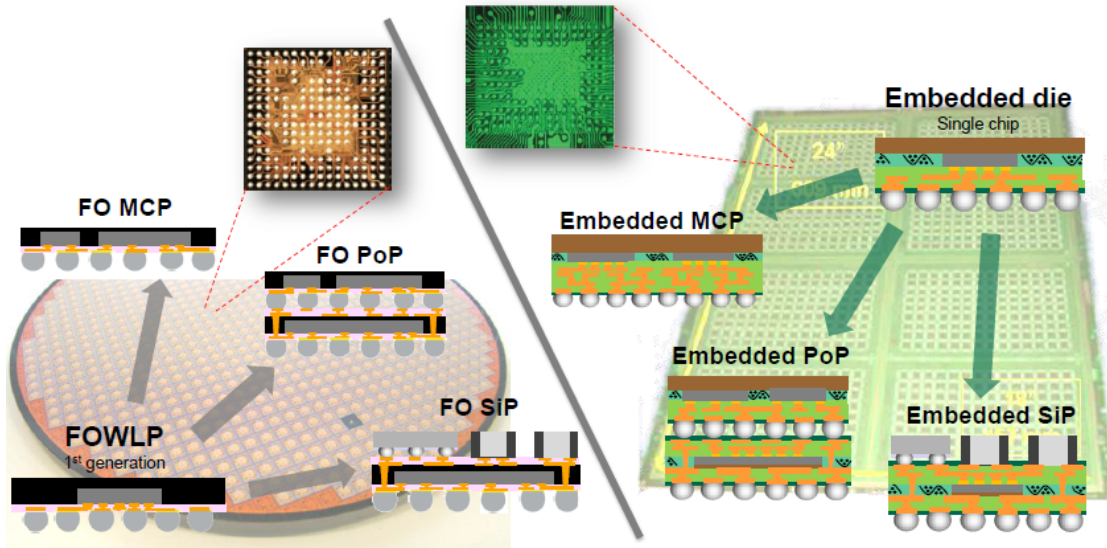


Figure 5: FOWLP and Panel processed Embedded Packages

Each of these approaches has their own strengths and challenges that are summarized in Figure 6 below.

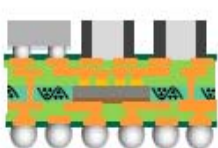

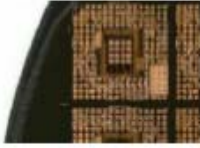
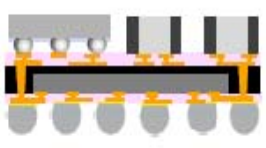
Overall Comparison Summary Between FOWLP / embedded die packaging infrastructures		
	  Embedded die	  FOWLP
Pros / Strengths	<ul style="list-style-type: none"> • Panel size PCB infrastructure → Low cost thanks to collective process + low cost BOM (specific selection of materials) • Already “3D”: possibility to immediately connect both sides of the Panel substrate • Thick Copper metallizations of PCB techno might be key to succeed in the high power components space (MOSFET, IGBT...) • Higher reliability expected on larger board size (> 12mmx12mm) • No issue of thin wafer handling , wafer bow / warpage 	<ul style="list-style-type: none"> • Infrastructure is clearly ramping in volume (> \$200M equipment investment the past 2 years) and growing fast on both 200/300mm • Supply chain is quite straight forward as the technology will be implemented and realized by the current packaging players (OSATs and IDMs) • No warpage issues as with organic substrates. Higher expected board level reliability than chip embedding / BGA / PoP for large footprints (above 40mm²)
Cons / Challenges	<ul style="list-style-type: none"> • Supply chain is complex: packaging value moving to PCB areas, that is totally new + need to establish company partnerships that are crossing-over the packaging, assembly & test supply chains • Lower rerouting density than front-end type of RDL (like fan-out). Line width/spacing today limited to 40x40µm, can go down to 25x25µm then 15x15µm in the future • Extra steps are required: WLP redistribution, Copper pads formation, thinning/ polishing, dicing and test • Manufacturing yield is low: typically 70 - 90% (need > 98%) • Standardization, Test methodology is not mature • Infrastructure is not developed enough yet to drive the cost down in the roadmap 	<ul style="list-style-type: none"> • Mainly technical issues need to be solved: die shift, board level reliability on large package sizes and thin wafer handling • Package size limitation: 8x8mm today, 12x12mm max in the future • New set of materials to be developed: mold compound, dielectric • Not “3D” yet: development of TMV “through mold vias” and double-side redistribution is highly needed to target SiP / PoP applications • Infrastructure only emerging on 200mm/300mm wafer size: need to rapidly move to PANEL size in order to lower cost and quickly expand in analog & mixed signal applications • Minimum bond pad with no need for redistribution on device wafer is 80µm. Need to improve tolerances
Conclusion	<ul style="list-style-type: none"> → Short term: introduction of the technology initially only in low-end, low I/O products: typically for “component level” packaging of power and analog applications (IPD, MOSFETs, RFID, etc...) → Medium term: Rapid expansion is then forecasted in simple, SiP module applications to benefit from 3D stacking & assembly capability (multi-die, integration of discrete passives) → Long term: Cost, yield and infrastructure will determine how far embedded die technology will expand 	<ul style="list-style-type: none"> → Short term: rather suited for “component level packaging” of digital chip IC applications with I/Os > 150- 250 at the beginning → Long term: With the burst ramp activity around eWLB infrastructure, the industry may favor FOWLP rather than embedding on substrate for logic LSI application most likely, or may even infiltrate some analog applications supply chain for FOWLP establish more rapidly than Embedded die in substrate

Figure 6: Comparison of embedded packaging categories

Both Panel and FOWLP based embedded packaging will be used with the PCB Panel base better suited to low end products with low I/O count. The FOWLP packaging is better suited to the more complex, smaller geometry products with tighter I/O since it incorporates the wafer level production precision and the Panel approach uses PCB Panel processing tools.

WAFER LEVEL PACKAGE DEVELOPMENTS AND TRENDS

Today, WLP developments are motivated by the recognition that wafer level processing technology, i.e., parallel processing on the wafer, opens additional alternatives to traditional packaging and assembly. WLP includes not only processing on active devices, but also processing of silicon dice with integrated passives, other substrates such as glass leading to wafer level substrates, and artificially reconstituted polymer wafers with embedded die.

For package substrates, fine design rules and the capability of creating integrated passive devices are attractive features. Dielectrics and traces are built on silicon substrate by wafer process technology and the following assembly is performed on the wafer level substrate. Some wafer level substrates are not made of silicon but dielectric layers and traces built up on a wafer, which will be removed during the manufacturing process.

Currently, different technologies at wafer level are in development to satisfy the need to increase performance and functionality while reducing size, power, and the cost of the system. This development leads to more complex packages for both single and multi-die Wafer Level Packages.

The wafer level CSP may incorporate copper post terminals with thicker resin coat providing a package that is more durable to the rough handling and more tolerant of CTE mismatch. This package is used for a variety of the applications from power amplifier to CPU with the ball pitches as fine as 0.20 mm.

The wafer level CSP specialized for image sensing is a glass-sealed optical wafer level CSP. Die are sandwiched or laminated on the circuit side by clear glass and terminals are routed to the reverse side of the die via TSVs or beam-lead metallurgy extending to the side of the die.

Low cure temperature polymers, with cure temperatures below 200 Celsius are being developed to allow the implementation of embedded flash into WLPs, insuring the integrity of the memory states during standard WLP processing. These lower cure polymers are also needed for fan-out packaging, as the mold compound used to reconstitute the wafers are typically epoxy based systems with relatively low Tg's. They also serve the special needs of WLP with TSV and IPD processing.

FUTURE TRENDS FOR WAFER LEVEL PACKAGING

Developments needed to meet the future requirements of wafer level packaging include:

- Continued reduction of processing temperatures, particularly for dielectric curing. This will require new material.
- Wafer-level substrates with passives in silicon or passives in RDL
- Integrating passive structures into the RDL by thin film dielectric deposition
- System integration at wafer level with silicon or glass wafers
- Embedded active and passive devices
- Wafer-level assembly—die to wafer—of Si (memory, MPU), MEMS, III/V (InP, GaAs, GaN etc.) and SiGe devices at wafer level
- Integrated shielding (RF and power)
- Functional layers integration (actuators, sensors, antennas)
- Through-silicon-via (TSV) formation and metallization, wafer thinning and adjusted bonding technologies for stacked dies on wafer (see Interposer and 3D Integration sections)
- Optical chip to chip interconnects
- TSVs on WLP to allow double-sided connectivity, including Package on Package (POP) applications for WLPs
- Continued development of WLP for mechanical MEMS, in addition to the current optical MEMS applications
- RF MEMS application for WLP (cavity protected by encapsulation material)

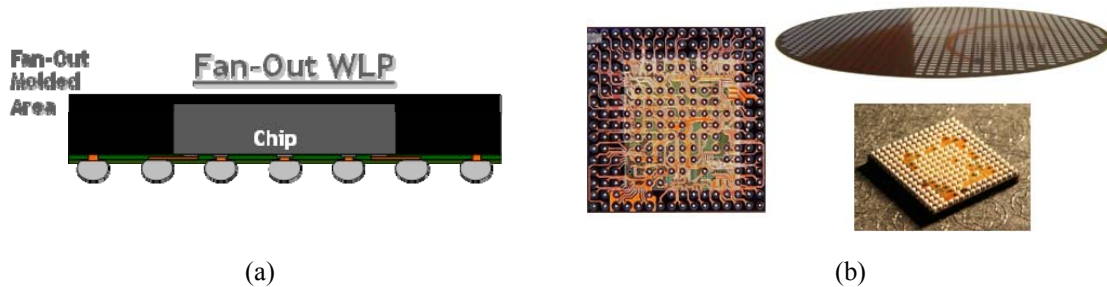
The development of wafer level packaging (WLP) is proceeding in several directions. These directions have shared requirements but each also has its own unique requirements. The directions include:

- Processes for larger die and higher functionality application based on RDLs (fan-in)
- Fan-out approaches (see various Embedded Wafer Level Package approaches)
- Higher complexity applications such as System in Package (SiP), 3D configurations and passive device integration. This includes face down and face up approaches on active Si devices, carriers with passives, etc. and potentially glass substrates.
- New applications such as multiple IC stacks (memories, processor-ASIC-memories, MEMS); based on through silicon via (TSV) technology
- Wafer to wafer stacks
- These WLP technologies are driven by market demand for higher integration density and system capability (See SiP section)

EXAMPLES FOR EMERGING WAFER LEVEL PACKAGE TECHNOLOGIES

FAN OUT WLP USING RECONFIGURED WAFER LEVEL TECHNOLOGIES

New package developments that have begun production and in consumer products are fan out or embedded wafer level package technologies. These technologies allow higher integration density and fan-out solutions using WLP technologies. For this new approach the chips are reconstituted and embedded in an epoxy compound to rebuild an artificial wafer. A thin film redistribution layer is applied (Figure 7) instead of a laminate substrate, which is typical for classical BGAs. Laminate substrates are reaching their limits in respect to integration density at reasonable cost. Thus, the application of thin film technology as redistribution layers opens new opportunities for SiP. The possibility to integrate passives, like inductors, capacitors or even active devices into the mold compound or various thin film layers opens additional design possibilities for new SiP. There are other approaches that incorporate a copper pillar over ball-integrated arrays. Special difficult challenges for these types of embedded wafer level packages are their implementation in the packaging industry infrastructure from design to manufacturing, and surface mount assembly to the board and board level reliability. These packaging technologies will require closer cooperation between the die design and packaging engineering groups to insure the manufacturability of the entire die/package structure. This will minimize the packaging cost and maximize the manufacturing yields.



Graphic courtesy of ASE

Graphic courtesy of Infineon

Figure 7: *Wafer Level Packaging*

DIFFICULT CHALLENGES FOR WLP

Wafer level Packages are expected to have better reliability even for larger die with small ball pitch. The physical structure and the materials used are being refined to satisfy the requirements of specific applications. This is a particular challenge for MEMS devices.

Key challenges include:

- Board level reliability especially for large die
- Testing of wafer level stacked packages and new 3D architectures with multiple die
- Vias through chip (WLP) and package (for embedded wafer level architectures)
- Thin package profile using very thin silicon die for extremely thin applications
- Mechanical tolerances required for chip alignment to small pads
- Contacts on small pads
- High reliability (electromigration, drop test)
 - Thick copper post structure materials for better resistance to electromigration
 - New solder material for low temperature Pb free and greater strength
- No solder interconnection
- Topology of multilayer RDLs
- Heterogeneous integration of different materials—dielectrics, conductors and semiconductors—with mismatch in CTE, interfacial adhesion, stress tolerance, etc....
- Topology of thick metals for high current and/or improved conductivity materials
- Reduction of metal roughness for RF (skin effect)
- Cross talk on chip because of small vertical distance
- Yield and defect repair possibilities for embedded WLP products

6. 2.5 D INTEGRATION

The use of silicon interposers for advanced packaging, first introduced as a product by Xilinx, is now in use for 2.5D integration. The introduction of product with 2.5D integration used a TSV interposer to connect multiple chips side by side and provide high bandwidth connections between the die, RDL to map the die geometries to the printed circuit board geometries and TSVs to connect the top and bottom layers of the interposer. This is illustrated in Figure 8 below.

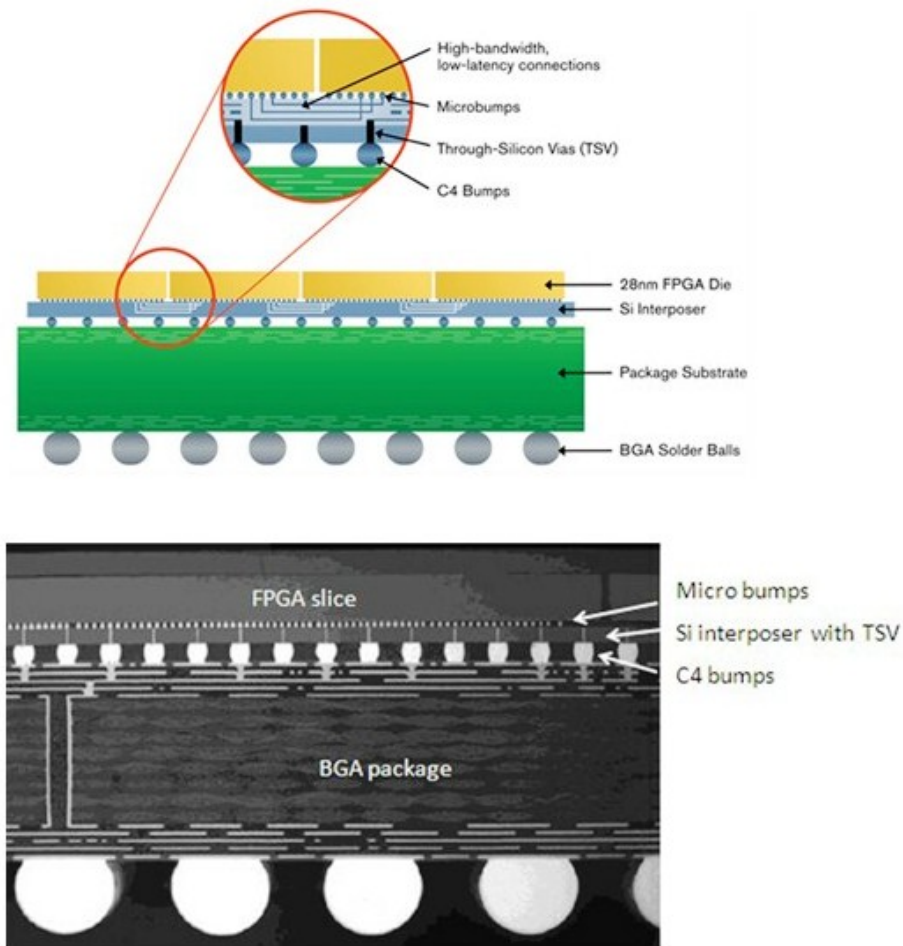


Figure 8: 2.5D Interposer for Xilinx FPGA

The benefits of higher bandwidth, lower power and reduced latency are compelling and several other products are in development using this technology. This package element is also in use as a substrate for 3D integration. The key technical parameters for interposers are in Table HI-16. The table addresses both base silicon interposers used for 2.5D architectures and intermediate silicon interposers used for use in a 3D stack. While silicon is the material of choice today, work is underway to use glass, ceramics or

polymers for interposer material. Each approach has some potential advantages but for now we have addressed only silicon and glass.

The initial selection of this packaging technology was driven by the need for improved performance and it was very successful in achieving that goal. Nevertheless the widespread adoption of this technology has not followed. The primary limitation was the high cost of the interposer incorporating TSVs. Driving the cost down for the 2.5D technology is a critical challenge since it not only delivers major performance advantages, it also drive the industry down the learning curve for the cost effective adoption for 3D-TSV.

7. 3D INTEGRATION

The limits of Moore's Law scaling are already evident. The technical challenges of scaling as we reach the limits of the physics are difficult which is slowing the pace and increasing the cost of scaling. In addition, the benefits of scaling are reduced since scaling in size is not matched by the historical performance advantages. The effort to continue the pace of progress for the semiconductor industry has been focused on two technical directions. Functional diversification which is referred to as "more than Moore" is one direction and for packaging. It is the driving force behind System-In-Package (SiP) architecture. The second is the use of the third dimension. This allows increase in functional density for a given node and also improves performance and reduces power requirements. This section addresses the requirements, difficult challenges and potential solutions to continue the pace of progress in performance, functional density and cost through use of the third dimension. There are several driving forces for 3D integration. The potential benefits include higher performance, reduced power requirement, reduced latency, smaller size and eventually lower cost compared to 2.5D and conventional 2D packaging. Some of the basic driving forces for 3D integration are presented Figure 9 below.

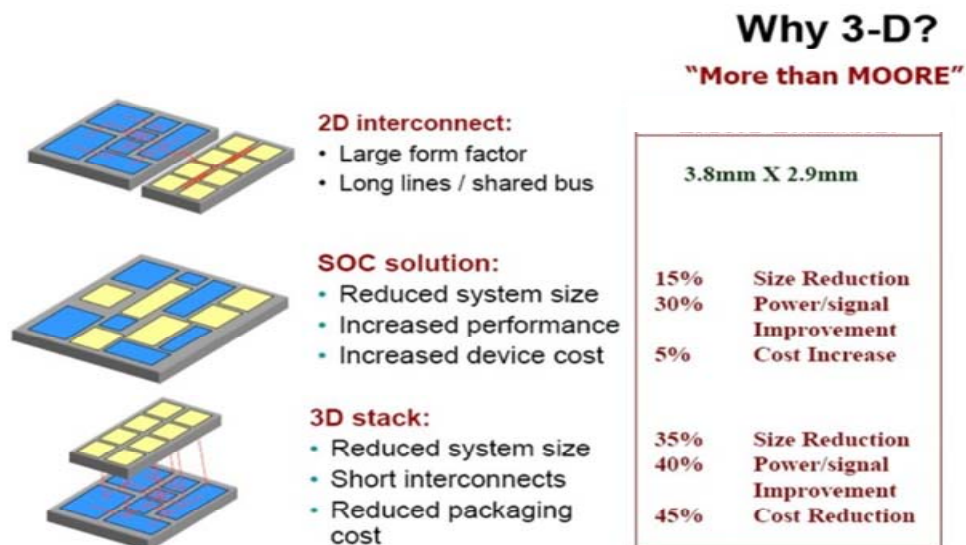


Figure 9: Driving Forces for 3D Integration

The result from combining these two technical directions to produce a complex 3D SiP provides the full benefits of both. The first high volume 3D SiP was for wide I/O memory modules. The advantages realized of increased bandwidth and reduced power through use of TSVs, copper pillars and are shown in Figure 10.

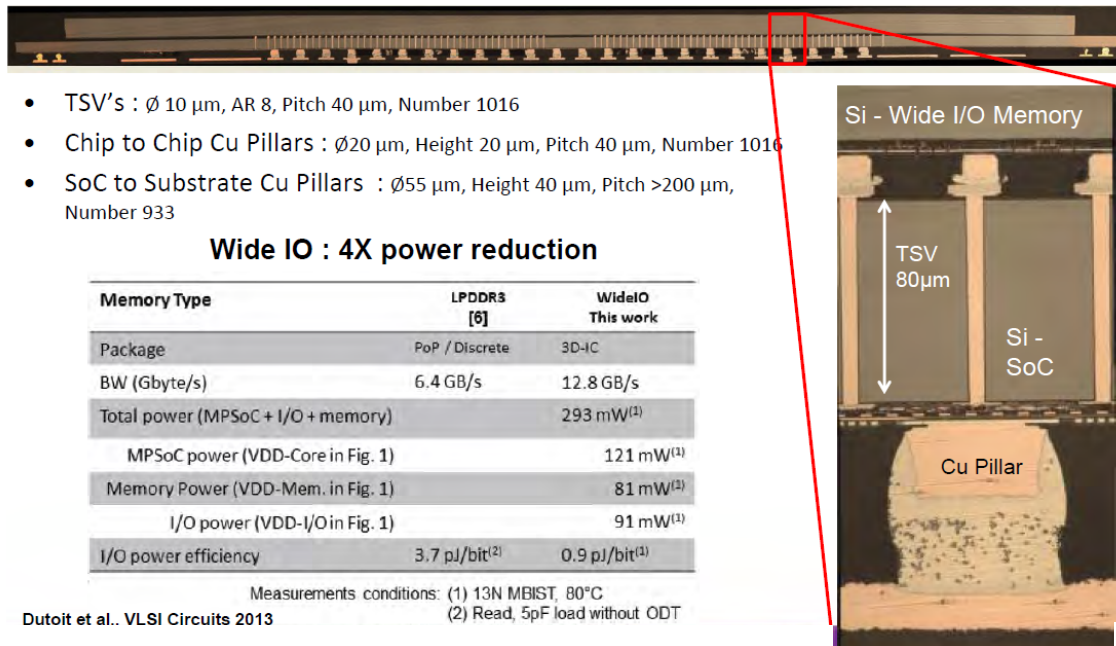
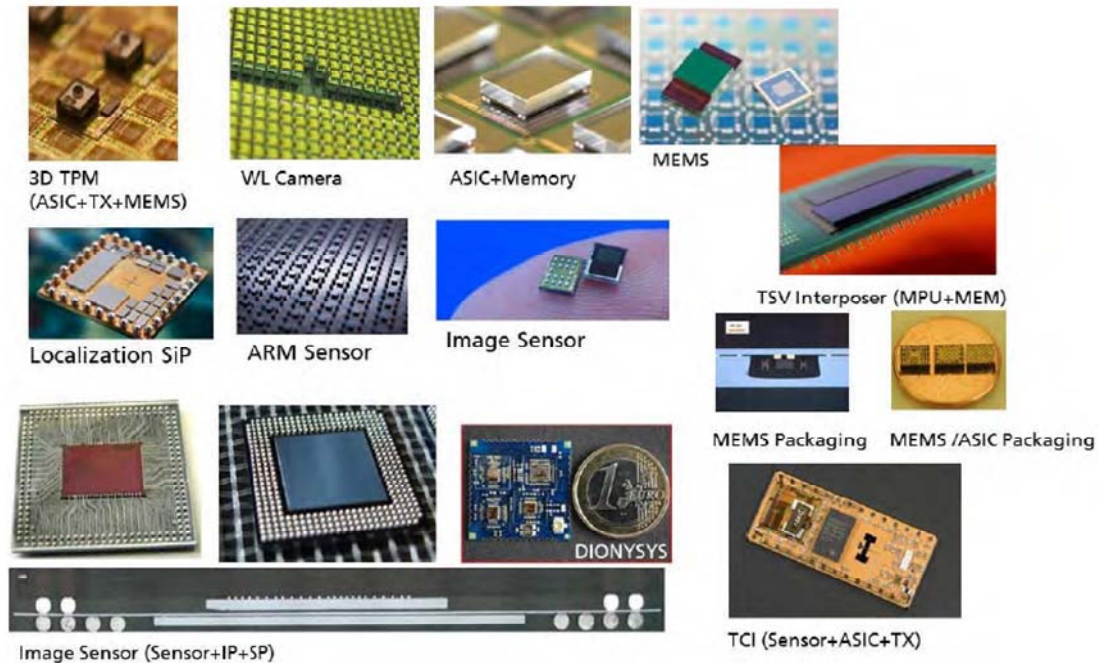


Figure 10: 3D-SiP for wide I/O Memory module with SoC.

There are a number of difficult challenges to achieve high volume production for 3D integration and maintain low cost. Innovation in processes such as wafer thinning, alignment accuracy, low temperature bonding, microfluidics, MEMS integration and Microphotonics will be required. The materials available today are not adequate to meet these challenges and some must be replaced. This section will focus on the specific 3D integration issues. Specific details of new materials and processing technology are addressed in other sections of this Chapter.

There is a separate section following that addresses the thinning processes required for 3D integration. Many difficult challenges remain related to cost, reliability, alignment accuracy for D2D, D2W and W2W, and bonding techniques. Despite these challenges Consortia of industry and academia working on this subject are making rapid progress. Volume production of TSV based product has already commenced for limited applications such as mobile phone camera modules, memory modules and high-end 2.5D products. The broad use of this technology will begin as the industry comes down the learning curve thereby reducing cost.

Many examples exist for 3D integration as illustrated in Figure 11 below.



Source: Fraunhofer IZM
 Figure 11: Examples of 3D SiP Integration

The examples above include heterogeneous integration of diverse components including analog devices, memory, logic, RF and a variety of sensors. All of these devices have been packaged and proven; several are in volume production today. These examples combining heterogeneous integration for SiP packages and 3D integration are essential for packaging to maintain the pace of progress.

DIFFICULT CHALLENGES FOR 3D INTEGRATION

The difficult challenges and potential solutions for 3D integration are listed in table HI-19. 3D integration is now in high volume production for memory modules and camera modules and several others are entering the market or in production now at lower volume. The greatest challenge is to meet the cost requirements. Progress in wafer thinning, TSV fabrication and wafer/die bonding has significantly reduced cost and it will continue rapid improvement as we come down the learning curve with high volume production experience.

3D INTEGRATION DEFINITION OF TERMS

The definitions of terms for elements of 3D integration used in this section are illustrated in Figure 12 below.

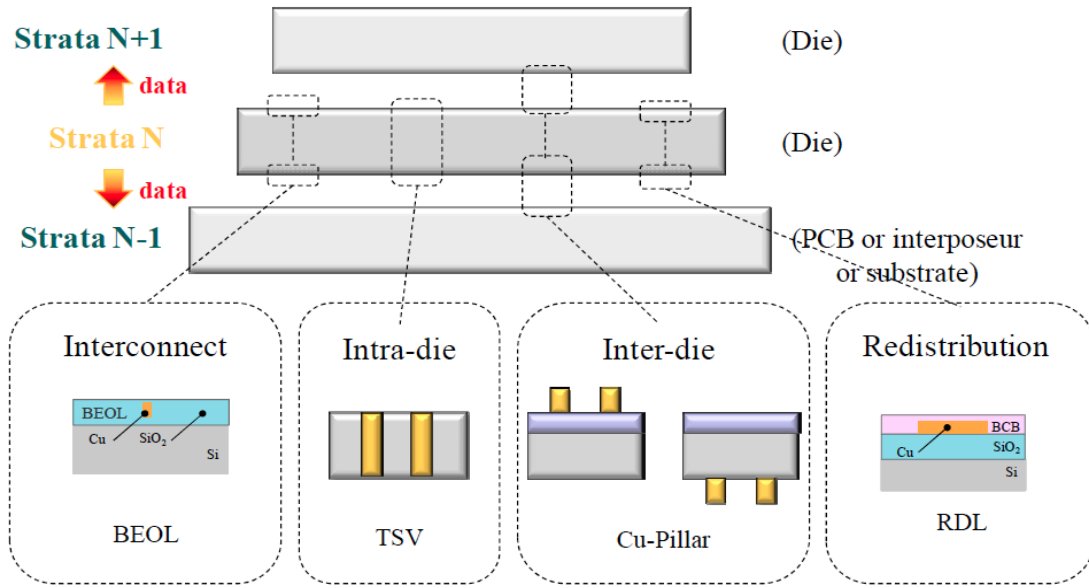


Figure 12: A schematic of 3D integration. Source: IEEE ECTC 2015

An example of process flow and equipment requirements is presented in Figure 13 below.

PROCESSES FOR 3D-TSV INTEGRATION

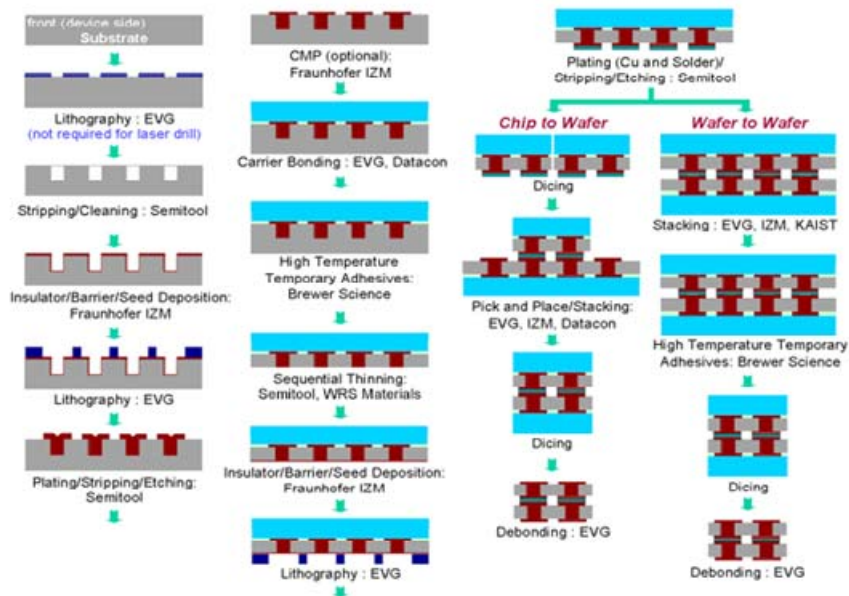


Figure 13: Example of Process flow and typical equipment for 3D integration.

Equipment exists to support this process flow but new equipment with improved alignment, improved process control and higher throughput will be required to meet future targets for feature size, layer thickness and cost.

TECHNOLOGY REQUIREMENTS

The major new packaging technologies for 3D integration are:

- TSV formation for via middle and via last (via first is addressed in the interconnect chapter)
- Wafer thinning
- Handling of thinned wafers and thinned die
- Bonding and interconnect (at low temperature)
- Package substrates with high wiring density
- Formation of package enclosures (particularly for MEMS and Photonics elements)
- Thermal management
- Power integrity in the stack
- Redundancy and continuous test while running, etc.
- Micro bump formation

TSV FORMATION

There are 3 processes used for TSV formation defined by where they lie in the process flow; via first, via middle or via last. The “via first” process is addressed in the Interconnect Chapter and via last is used only in special cases. The via last is formed after all front end processes have been completed and generally requires very large via diameter, very high aspect ratio or both. These 2 process flows are illustrated in Figure 14 below and will not be addresses in more detail in this Chapter.

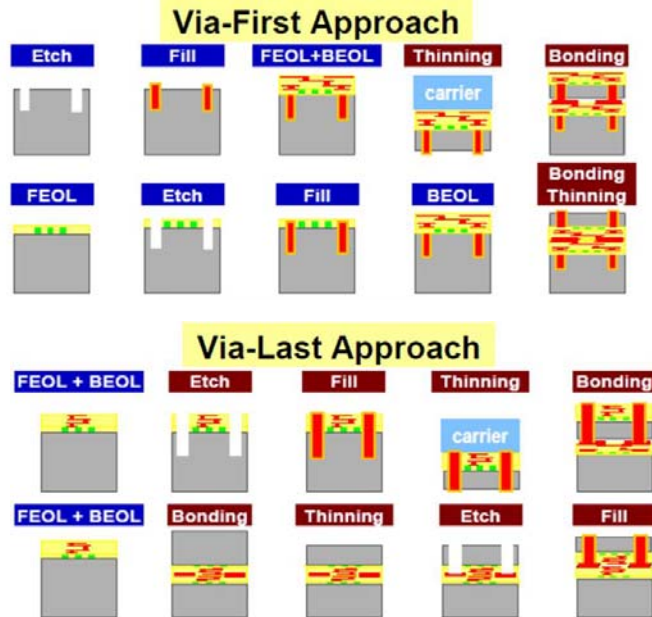


Figure 14: Process flows for via first starts before CMOS FEOL and via last starts after CMOS BEOL

The process that is dominant in IC foundries today is via middle due to cost and performance issues. A process flow for via middle is shown below (Fig. 15).

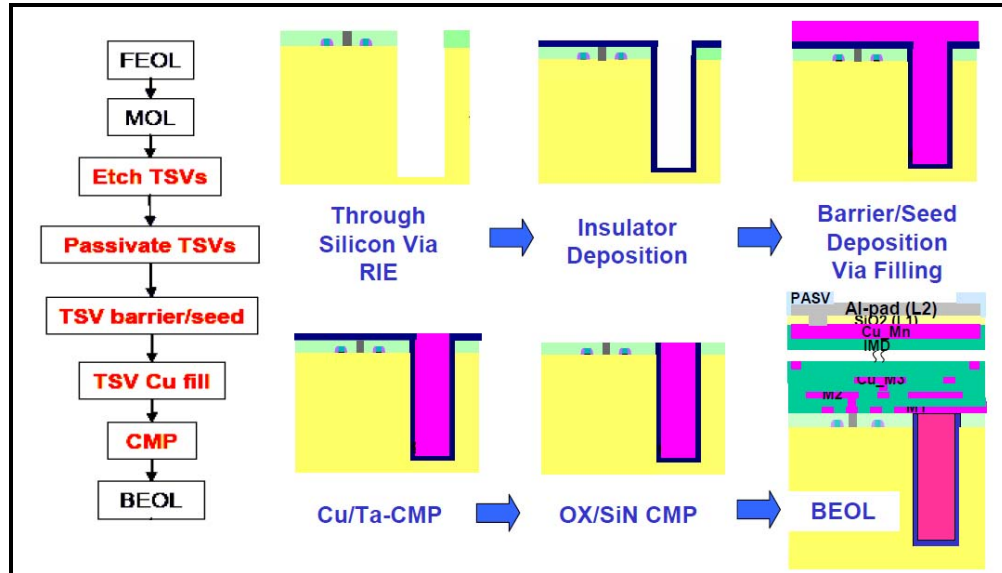


Figure 15: Via middle TSV Process flow is inserted between FEOL and BEOL CMOS processes

TSV INTERCONNECT METHODS

The process technology for TSV formation is fairly well established. They are now manufactured in high volume for camera modules and they are in production for 2.5D interposers with other applications in development. There are a variety of stacking interconnect methods for different applications that are addressed in Table HI-18.

The basic processes for the TSV formation are via etching (DRIE, laser), insulation, and metallization, which are well known from front-end processing. Additional processes that are required for the stack formation are wafer thinning, deposition of redistribution layer (RDL) and under-bump formation, wafer level bonding processes (die-to-wafer or wafer-to-wafer), as well as final encapsulation.

Key technical challenges for the TSV approach are:

- High density and high aspect ratio via etching
- Low temperature processes for passivation and metallization
- High speed via filling (e.g., electroplating (Cu), CVD (Cu, W))
- Thinned wafer/device handling
- High speed and precise wafer level alignment and assembly processes (die-to-wafer and wafer-to-wafer)
- Testing and methodology
- Competitive cost

The first applications of TSV are in production today for CMOS image sensors and stacked die for memory devices are in production today.

WAFER/DEVICE STACKING

The key technical parameters for stacking architectures are summarized on Table HI-17. A variety of options have been proposed for the actual stacking of die, and packaging of

the stacks. The three common categories of bonding are thermocompression, reflow and direct bonding illustrated in figure 16 below:

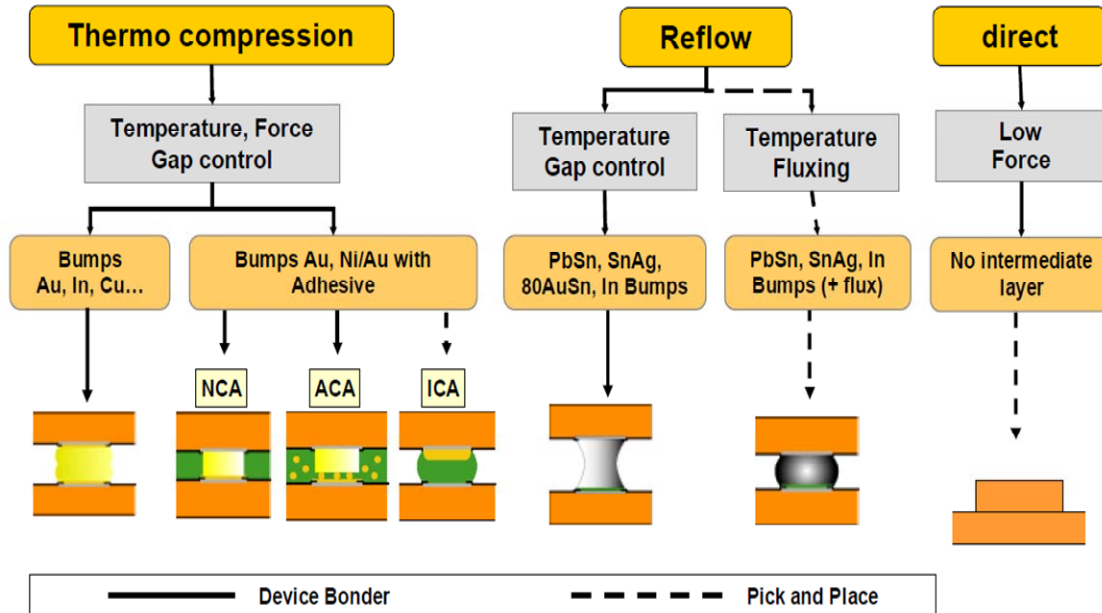


Figure 16: Die bonding processes for bonding D2D, D2W and W2W

The relative merits of these bonding approaches for stacking, with the process requirements of high assembly yield, low complexity and low cost, will point to die-to-die (D2D), and die-to-wafer (D2W) stacking until progress on standards and alignment accuracy allow wafer-to-wafer to be adopted. The choice will be determined based on application and economic grounds.

For die-to-die and die-to wafer stacking, the industry is focused on micro-pillar or micro-bump interconnect methods. The advantages include high throughput if a mass reflow process can be used and compatibility with the conventional flip chip interconnect methods.

Wafer/Device stacking today is typically done with relatively thick layers that may be handled by standard methods. As stacking layer count rises the layer thickness will decrease and cost effective solutions to handling very thin layers down below 20 μ m will be needed. The technologies for thinning and handling very thin wafers are addressed in section 11 of this Chapter. A further challenge presented by HI is the potential requirement of stacking of layers of different materials. This is unlikely for W2W but is a potential solution for integrating optical and electrical elements using D2W stacking.

For wafer-to-wafer stacking, the industry is currently focused on two bonding methods:

- Direct interconnect bonding (DIB) which uses the preferred foundry-based TSV technology and has the advantage of simultaneously forming the electrical bonds, and oxide bonding.
- Copper-copper thermocompression bonding is very slow (~8 bonds/hr in a four-chamber tool).

DIB is capable of performing 25 bonds/hr in a single-chamber tool. With a high alignment accuracy of better than 1 μm , which is expected to be in the sub-0.5 μm range within the next one years, interconnect pitches of 6–10 μm can enable high interconnect densities of ~1–3 million interconnects/ cm^2 . For the next 2–3 years, alignment capability will not be the bottleneck.

Oxide diffusion bonding (direct bonding) is 3 \times faster than copper bonding. However, the electrical interconnect is formed after the bonding, thus requiring an extra process step and potentially a level of complexity.

In addition to the bonding techniques needed and various wafer/device stacking configurations, the stacking sequence and the coupling with the TSV revealing (or protrusion) and packaging assembly processes are also critical to achieving high assembly yield. Tezzaron has pioneered wafer-to-wafer bonding with the tungsten (W) TSV to serve as the “Super Contact”. By firstly using a face-to-face, copper-to-copper bonding, and then followed by the TSV revealing and consequently face-to-back bonding, the 3D wafer stacking is achieved without using a supporting wafer [1]. For 3D heterogeneous integration, like integrating a CPU or GPU with a 3D stacked, high bandwidth memory cube on a silicon interposer or directly on top of the processor, it is required that the Known-Good-Die-Stacks (KGDS) are made available to the final module integrator. To make and deliver the KGDS, die stacking on a carrier wafer and then following by reconfiguration and probing processes are developed. Over-molding of the memory die stacks while still on the carrier wafer is also developed to improve the mechanical integrity of the 3D die stacks and test access ability [2].

Similarly, for the completed 3D IC stacking and packaging assembly flow, Chip-on-Chip-First (CoC-First), Chip-on-Substrate-First (CoS-First) and Chip-on-Wafer-First (CoW-First) processes are evaluated and developed. Each has its own advantages and disadvantages. From providing a completed end-to-end, turnkey solution perspective, the CoW-First process has been adopted by one of the major wafer foundry supplier [3].

MICRO BUMP FORMATION PROCESS

The undercut of seed layer is the big issue in micro bumps formation. (Figure 17) This phenomenon is well known in the case of using wet etching process for seed layer. This is caused by capillarity and local cell effect under UBM. The length of undercut is typically 3~5 μm at one side of each bump. Therefore, a new micro bump process (Figure 18) without wet etching has been developed with bumps less than 15 μm in diameter for 3D integration. It uses electro-less plating and a solder ball placement process. It has no wet etching process of seed layer.

Undercut issue of seed layer

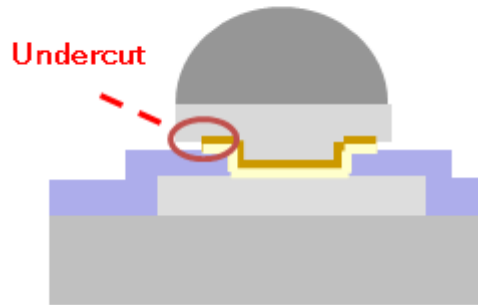


Figure 17: The undercut issue using wet etching process

Example of new process without wet etching

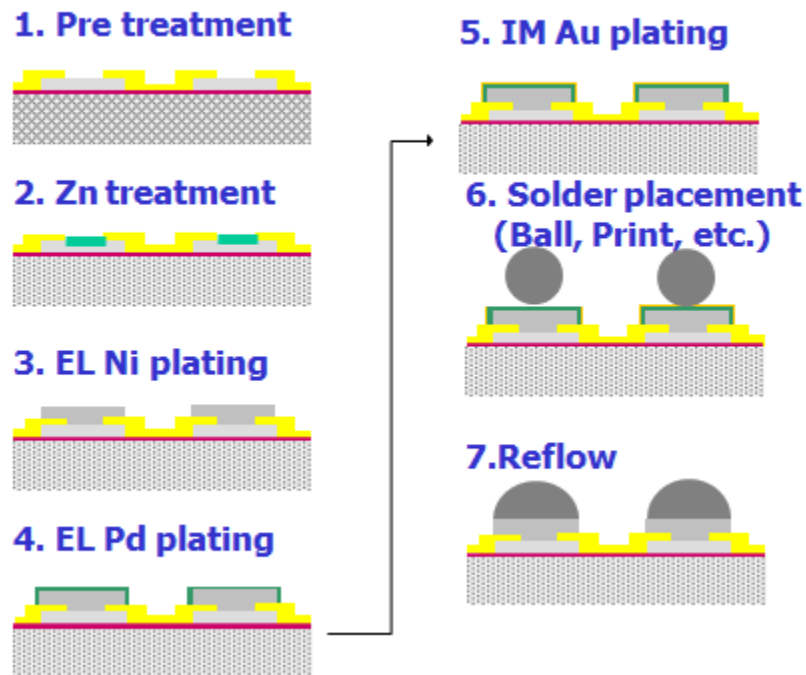


Figure 18: Example of new micro bump formation process without wet etching process

REQUIREMENTS FOR HIGH K DIELECTRICS WITH HIGH BREAKDOWN FIELD

In order to achieve the lowest possible power consumption logic and memory should operate at the lowest voltage that gives reliable performance. The inductance and resistance in the power delivery wiring can result in voltage sag associated with spikes in operating current. As operating voltage drops it will be necessary to maintain voltage within 20-30mV. The only practical method for 3D stacked die is to place decoupling capacitors close to the transistor. In order for this to be done with no increase in thickness a high k dielectric is required between stacked die and perhaps in the interconnect on the die. The required properties are low temperature processing (below 200C), very low leakage current and very high breakdown voltage. These dielectrics can then be used between power and ground traces on the die in the stack to form capacitors. Dielectrics used forming on chip capacitors today have a k value of about 4 that is too low to meet the requirement. A k value of 10 to 100 times higher is needed while maintaining the leakage and breakdown requirements. It must also be free of dielectric fatigue or other potential reliability issue. There is no material available today that satisfies this requirement and the Emerging Research Materials TWG is looking for a solution.

3D ISSUES

Intermediate interposers must perform the functions of the base interposer with the probability of requiring redistribution wiring to match the geometries of the die connected above with the geometries of the die connected below the interposer. The coming increase in the number of die in the stack and increased heterogeneous integration will require the interposer to take on more complex functions. The interposer represents potential solutions for many of the difficult challenges. (See SiP section 6 of this chapter)

- Thermal management can be addressed by incorporating microfluidic channels into the interposer to circulate cooling liquids.
- Integrated passives may be fabricated on the interposer to provide decoupling capacitors, inductors and resistors.
- A relay matrix may be fabricated on the interposer to allow TSV connections to be switched. This can support test access as well as switching in of redundant components in the stack in the event a failure is detected.
- BIST and BOST engines can be located on the interposer to provide for continuous test while running. Sharing these engines through relay switching may enable sharing this resource.

HETEROGENEOUS 3D STACKING PROCESS

Fan-out WLP 3DIC structure

The process technology for heterogeneous 3D stacking is important. The candidates of structure are developed using Fan-out WLP process, D2D process or W2W process. In the case of Fan-out WLP process, it's easy to make the through mold via and heterogeneous 3D stacking by using WLP, but it's not able to realize the wide band and low power consumption like D2D or W2W structure. This structure is illustrated in Figure 19 below.

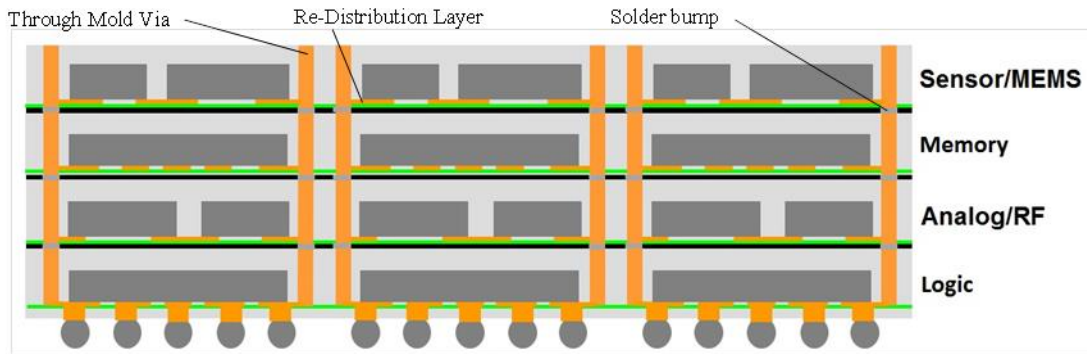


Figure 19: Heterogeneous 3D IC using Fan-out WLP process

D2D 3DIC structure

Another candidate structure is developed using D2D process (Figure 20). In the case of D2D process, its TSV cost is high and it needs long lead time to make the heterogeneous 3D stacking, but it's easy able to realize the wide band and low power consumption compare than Fan-out WLP process.

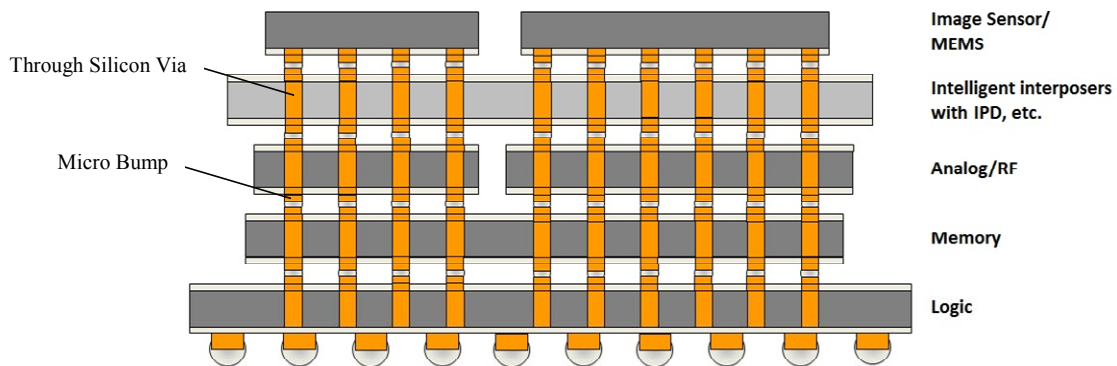


Figure 20: Heterogeneous 3D IC using D2D process

W2W 3DIC structure

The last candidate structure is developed using W2W process (Figure 21). In the case of W2W process, its TSV cost is of high and all chip size should be same, therefore it has big yield issue But it's not difficult to make the heterogeneous 3D stacking and is easy to realize the wide band and low power consumption compare than Fan-out WLP process.

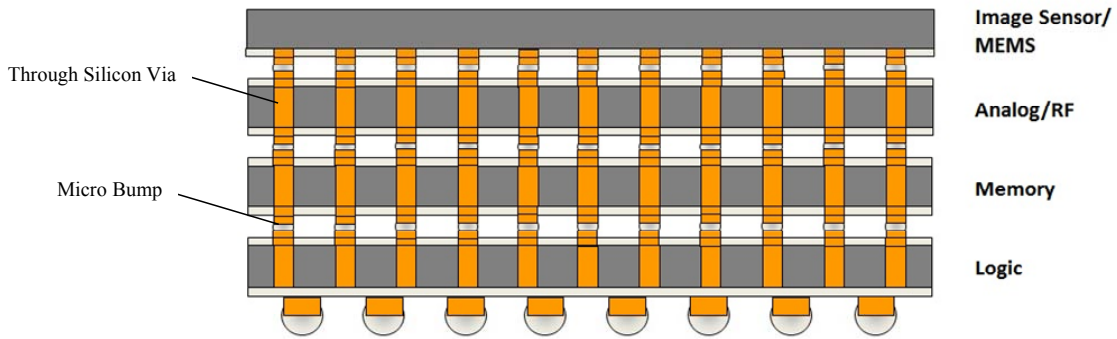


Figure 21: Heterogeneous 3D IC using W2W process

Regarding a heterogeneous 3D stacking process, all candidate processes have advantages and disadvantages respectively. Therefore, it needs to establish the best structure and process considering electric performance, process lead-time and cost.

EMERGING INTER-DIE INTERCONNECT AND BONDING TECHNOLOGY

An emerging Direct Bonding Interconnect technology commercialized by Ziptronix that was acquired by Tessera in 2015 supports W2W bonding at low temperature. The process follows standard back end of the line processes through oxide deposition and then inserts CMP and bond preparation of a plasma process followed by an ammonium hydroxide dip. The wafers are then aligned and joined at low temperature. The process is shown in cross section in Figure 22 below.

Cross-Section after Pick/Place (example)

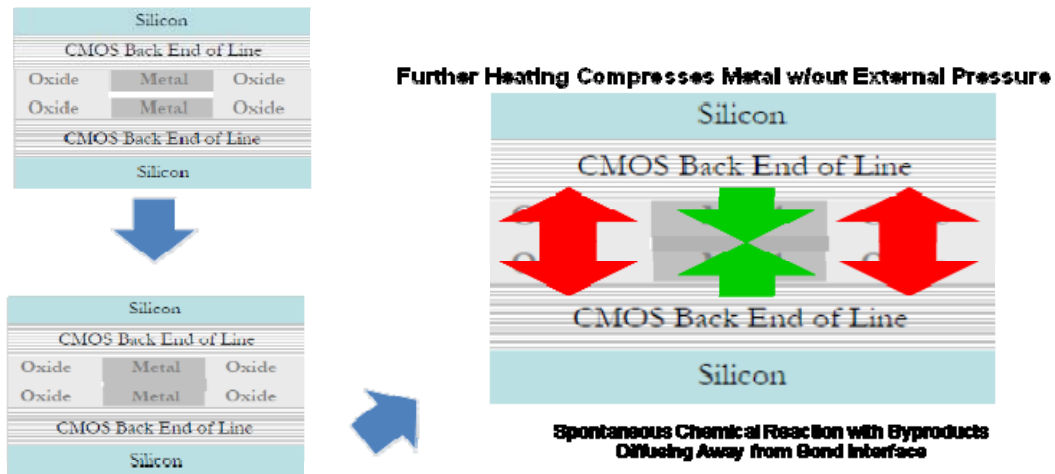


Figure 22: Face-to-face Direct Bonding Interconnect

The process is lower cost and higher throughput than traditional thermal compression bonding. This process has been demonstrated to have sub-micron placement accuracy and interconnect pitch below 10 μ m using conventional process equipment. The illustration above shows face-to-face bonding and face-to-back bonding is shown in the micrograph of Figure 23 below.

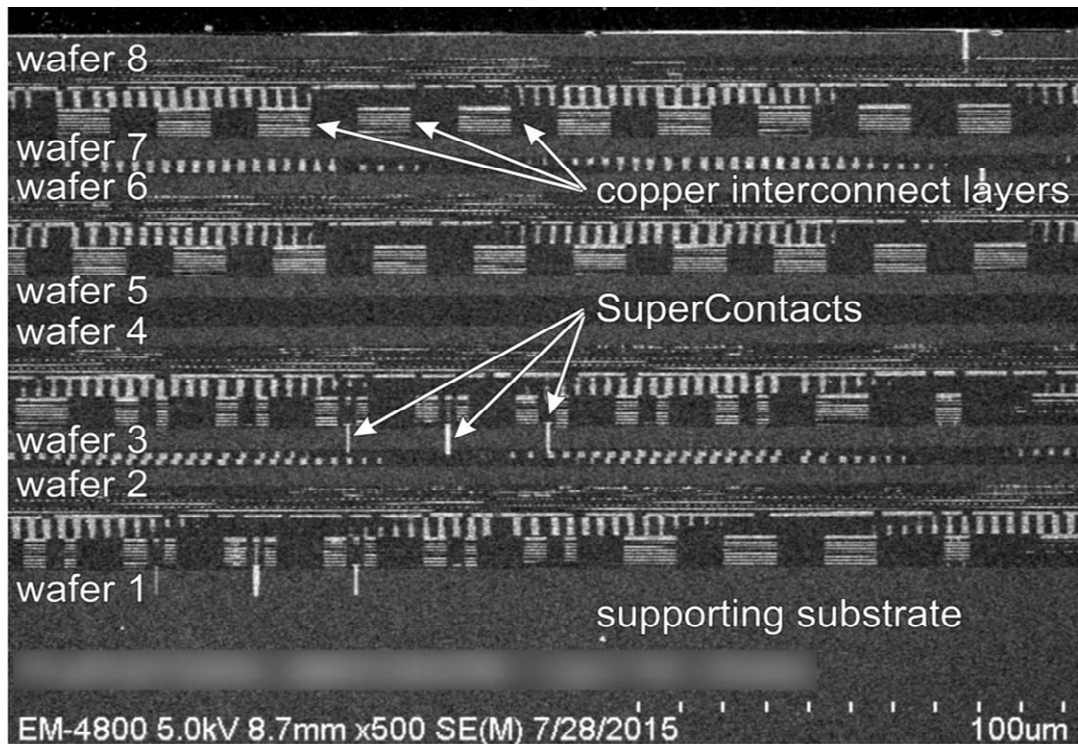


Figure 23: 8-layer active wafer stack from Tezzaron using DBI process

There are several other system interconnect methods that are potential solutions for manufacture of complex 3D SiP devices. Each has its own advantage and disadvantages and may be used for application specific solutions. Some of these methods are illustrated in Figure 24 below.

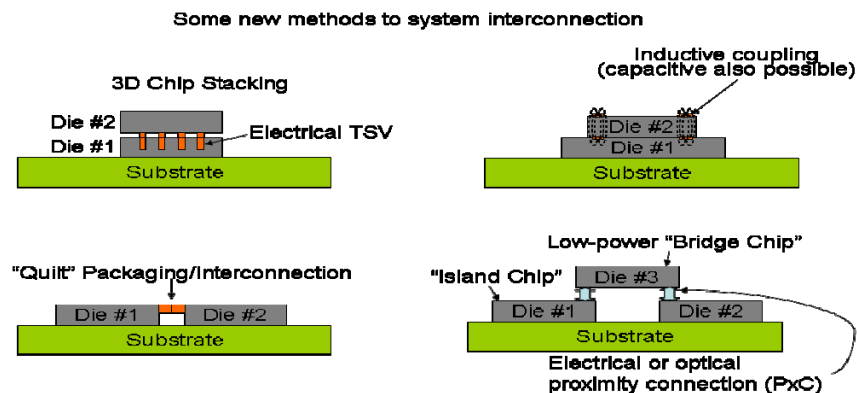


Figure 24: Methods of system interconnect for 3D integration

3D INTEGRATION OF LOGIC AND MEMORY

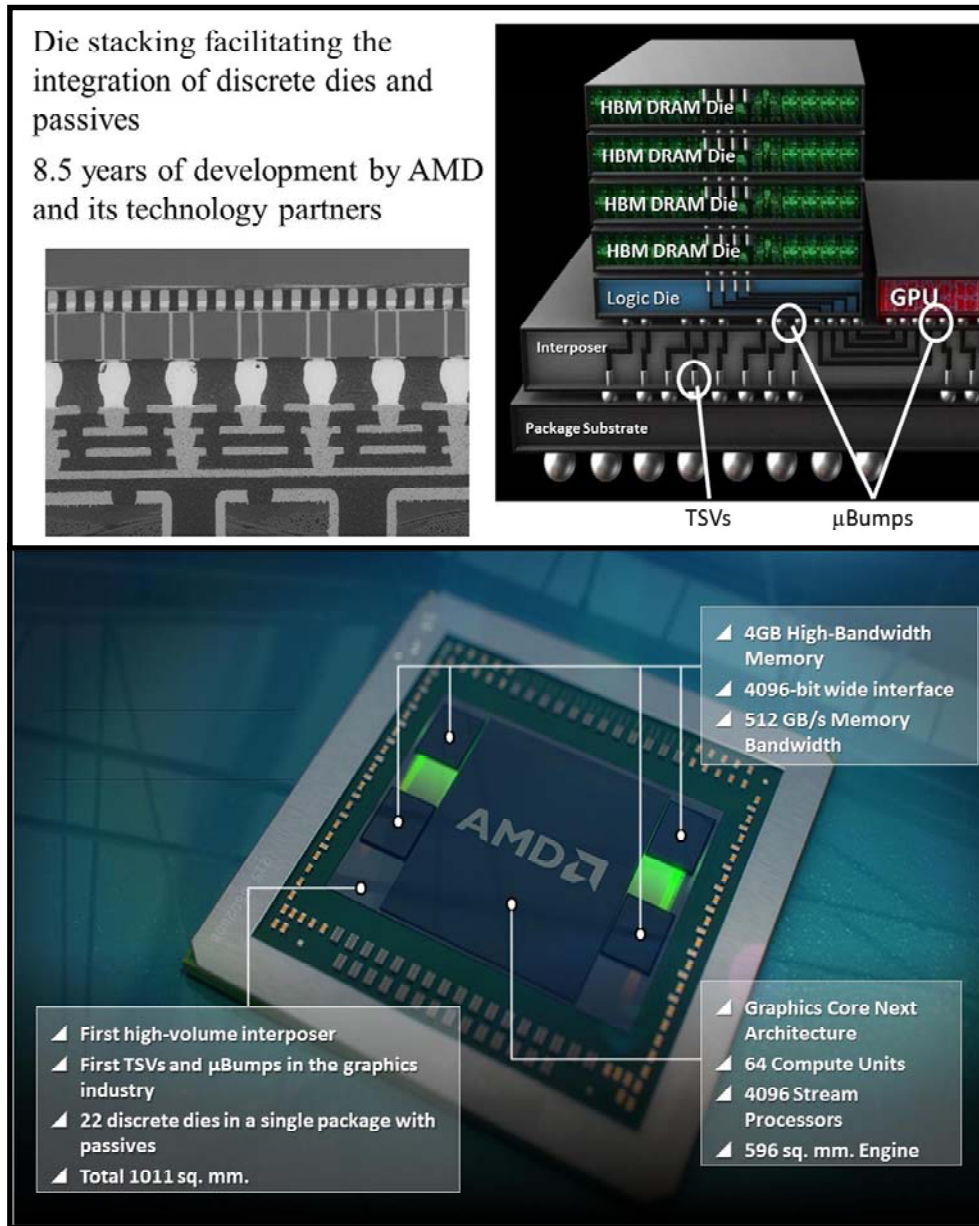


Figure 25: AMD Fiji product demonstrates advantages of 3D and silicon interposer technology

The 3D SiP product in Figure 25 incorporates memory, logic, passive components, a silicon interposer and delivers memory bandwidth of 512 GB/s. The interconnect structure in this package includes TSVs and micro-bumps. The next step should be the incorporation of photonics to the package that will reduce power and support increased physical density of bandwidth. The development of low cost photonic integrated circuits (PICs) is underway today and it will be incorporated in volume when they become cost competitive.

POWER INTEGRITY

The issue of power integrity for 3D-SiP packages becomes more challenging as the number of transistors rises and the operating voltages decreases. This is addressed in section 8 of this chapter.

THERMAL MANAGEMENT

While three-dimensional ICs provide low-energy and large bandwidth density signaling, thermal challenges in 3D can be significant and require careful design. In a single chip, heat can be readily accessed and removed from the back side (bulk silicon side) of the die. In 3D, when chips are stacked, there is no direct access to the back side of the chips in the stack nor a method of spreading the heat laterally from the stack. Thus, because of the increased power density after die stacking, high thermal resistance path for the embedded chips in the stack due to various low-thermal conductivity materials in the stack, maintaining all die in the stack at acceptable junction temperature may be difficult. The challenges in cooling are increased due to the fact that power dissipation is non-uniform across a die leading to the formation of hot spots.

In one study, it was shown that increasing TSV density in the region of hot spots can reduce peak temperature [26]. Increasing the thermal conductivity of the chip to chip interfaces within the stack would be beneficial in 3D thermal management. For that, metal bumps for thermal conduction purposes and high conductivity underfill material are some of the important considerations. For high power applications, improving the thermal conductivity path may not be sufficient, which has caused researchers to explore embedded thermal cooling technologies within the stack. For example, the use of embedded microfluidic heat sinks within the chips in the stack has been demonstrated in both academia and industry [27–28]. In one study, liquid cooling of a two tier $100\text{W}/\text{cm}^2/\text{tier}$ chips shows junction temperature of less than 50°C per tier [27]. However, one of the challenges with embedded microfluidic cooling in a stack of chips is the need to integrate TSVs within the relatively thicker silicon layers (silicon layer may increase due to the thermal resistance and pressure drop design requirements of the microfluidic heat sink).

Recent work on microfluidic cooling integration in a 3D stack has focused on the use of micropin-fin based heat sink (MPFHS) [29] along with TSV integration; a sample process flow is shown in Figure 26. The fabricated TSVs are $\sim 13\ \mu\text{m}$ in diameter and $\sim 300\ \mu\text{m}$ deep. The process flow for manufacturing this structure is shown in Figure 27 and SEM and optical images of the fabricated MPFHS with integrated copper TSVs are shown in Figure 28.

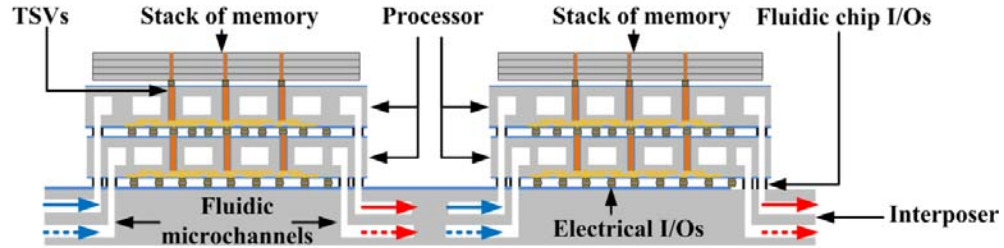


Figure: 26. Illustration of 3D IC system enabled using TSV-int within-tier microfluidic cooling technology.

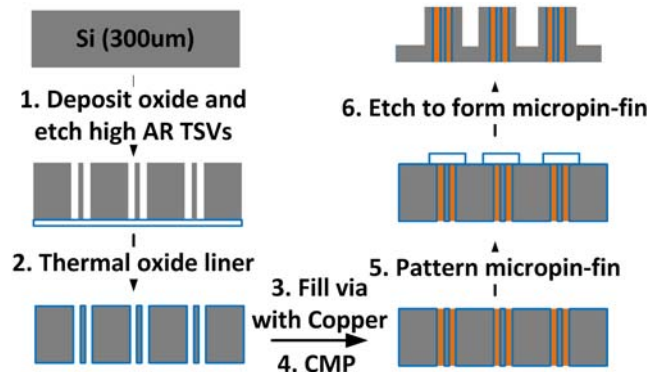


Figure 27: Illustration of process flow of high aspect ratio TSV integrated into the MPFHS.

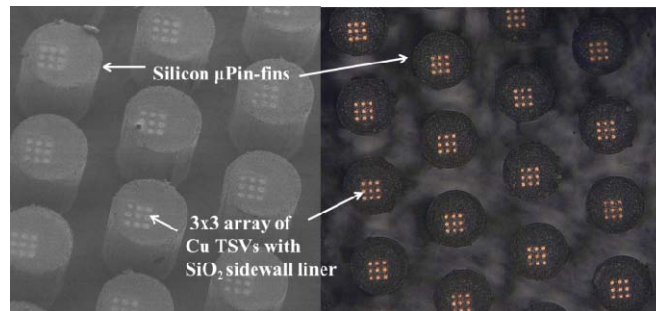


Figure 28: SEM (left) & optical images (right) of high aspect ratio TSVs integrated in micropin-fins (10 μm diameter, 35 μm pitch and 178 μm tall).

Power delivery is another challenge for 3D ICs. Power supply noise (PSN) results from current flowing across the parasitic resistance and inductance of the power delivery network. Multi-die stacks require high currents, and TSVs introduce higher resistance and inductance to the power delivery network. Thus, power delivery becomes more difficult for 3D ICs.

To address this need, electrical and fluidic microbumps have simultaneously been developed to enable high-bandwidth die-to-die signaling, embedded microfluidic cooling and power delivery for silicon interposer and 3D-based integrated systems. Figure 29 shows the external support required for this structure. The system works but its size and

cost prevent it from being a successful high volume solution. This represents a potential solution but significant research in process today will be required to make it viable.

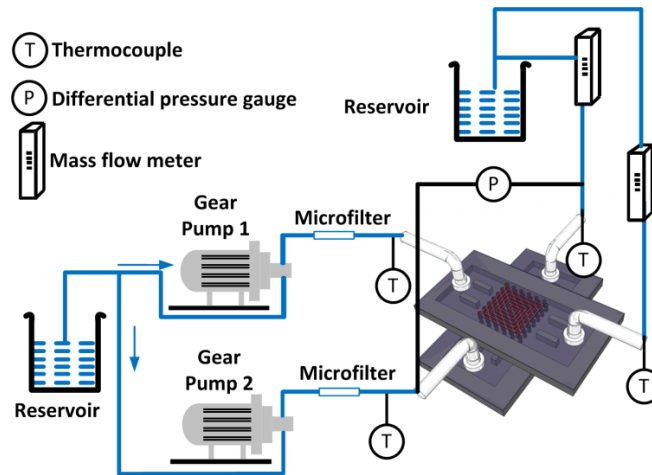


Figure 29: Schematic of the microfluidic test setup for testbed 1.

Figure 30 illustrates the fabrication results of high-density electrical microbump array (150×150 micron pitch) and two rows of fluidic microbumps. The diameter of the electrical microbumps is $50 \mu\text{m}$, and the inner diameter of the fluidic microbumps is $100 \mu\text{m}$. Chips and interposers with electrical and microfluidic I/Os have been successfully assembled using a conventional flip-chip bonder.

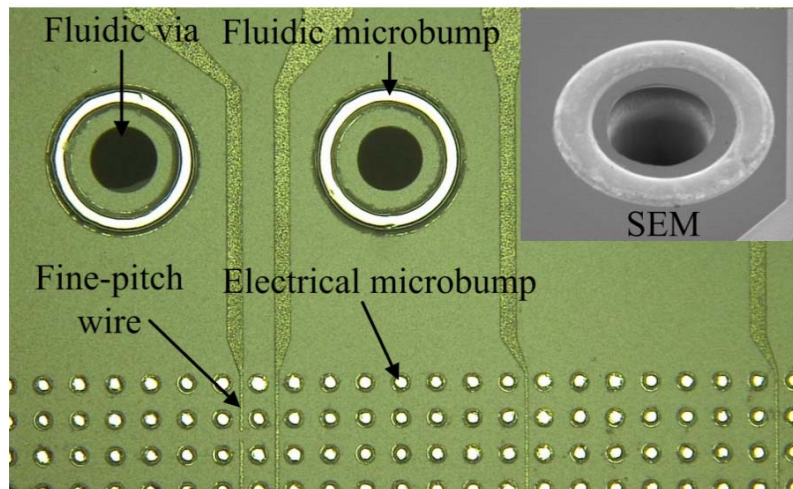


Figure 30: Electrical microbumps, fluidic microbumps, fluidic vias and fine-pitch wires

TEST FOR 3D INTEGRATION

Test access for 3D package architectures is sometimes not available with current technology. New methods to ensure functionality and reliability will be required. The solution will require access points to be designed into the package design at the die stack level. The inclusion of built in self-test (BIST) and built off chip self-test (BOST) elements will also need to be incorporated into the package.

The test requirement is dramatically increased by the fact that transistors at the smallest nodes will wear out. The Roadmap projects transistors count in the hundreds of billions for complex 3D SiP packages and even a very slow wear out rate may prevent the adequate reliability. This requires not only ensuring proper function when a package is initially completed but also some mechanism of continuous testing and self-repairs. Package designs will have to incorporate test elements to ensure reliability of complex systems over their design life. 3D testing is addressed in more detail in the Test Chapter.

RELIABILITY IN 3D INTEGRATION

3D chip stacks will experience the same environmental, mechanical and electrical stresses as in single chips during operations. However, in the 3D chip stack, there are extra silicon layers, called strata and TSVs, which add more structures and complexity to the system. The additional level of electrical interconnections introduces new failure opportunities and mechanisms for the 3D system. For example, mechanical stress, which modulates device mobility and V_t , can have negative impact on the performance of certain field-effect transistors (FETs). Similarly, the combined use of ELK dielectrics in BEOL with harder interconnect materials used in packaging (such as Cu pillars or Pb-free interconnects) is exacerbating Chip-Package Interactions (CPI) that cause delaminating, cracking and or fracturing of various materials that often limit yield and reliability for advanced packages. The increased power density and thermal gradient in vertical and horizontal directions related to TSVs and stacking of thin dice can also create unique reliability issues. It's very important to identify, evaluate and understand the reliability implications associated with 3D integration [30].

To manage the stresses in the 3D system, a Design-for-Manufacturing and Design-for-Reliability methodology needs to be implemented. Design rules that include properly defined TSV keep out zones and thermal-aware design flow should be part of the design environment for the 3D design tools.

To improve the yield and reliability of the 3D chip stacks, Built-in Self-Test (BIST), redundant interconnect structures and In-field repair mechanisms at the transistor and interconnect (including TSV) levels are needed. For example, a simple but effective solution is to add redundant TSVs that can be used to replace failed TSVs. This idea has been realized in 3D DRAM designs [31].

8. SYSTEM LEVEL INTEGRATION IN PACKAGE (SiP)

System level Integration in Package is not new. In one form or another, packaging engineers have been designing and assembling active and passive components in a single package for cost advantage, miniaturization and functionality. With CMOS scaling, device engineers have been able to increase the number of functions on a single chip (SOC) with each node introduction. Predictions that Moore's Law has reached its limits have been heard for years and have proven to be premature. While we are not yet at the physical limit of CMOS scaling, the economic advantage of scaling has been fast eroding. The ultimate end of Moore's Law scaling will be an economic question rather than a technical one. The convergence of escalating cost of mask sets, advanced nodes process complexity, and multi billion dollars cost of a new foundry, has led the industry to realize the price elastic growth of the industry cannot continue based on Moore's law scaling alone. At the same time the consumer market requirements for more functions such as Analog/RF, Passives, Power Devices, MEMs and Sensors, Optical components, Biochips and other calls for integration of those functions at the package level. The elements of a complex heterogeneous SiP depend on integration of diverse packaging technologies and packaged components configured to meet the requirements of each application. This is illustrated in Figure 31 below.

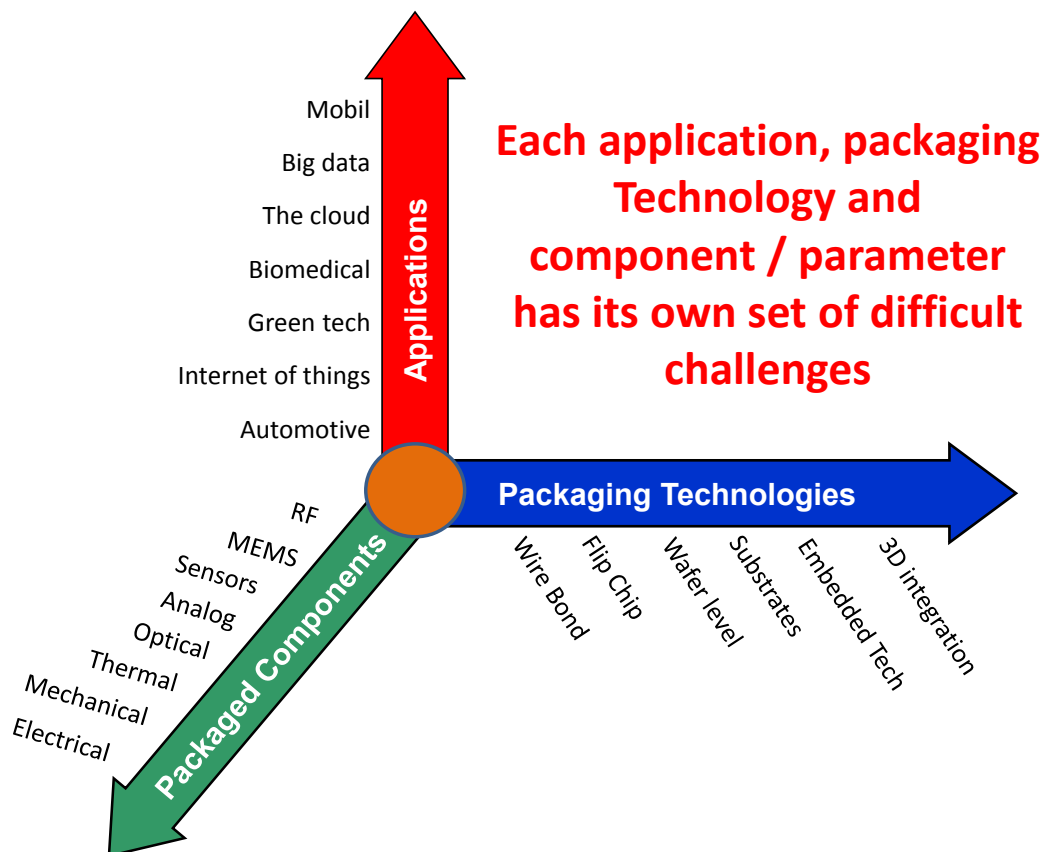


Figure 31: Elements incorporated into complex SiP packages through heterogeneous integration

This will require “More than Moore” heterogeneous integration through the tighter integration of system level components at the package level.

In the past scaling geometries enabled improved performance, less power, smaller size, and lower cost. Today scaling alone does not ensure improvement of all four items. The technical requirements for SiP are presented in Table HI-14. The primary mechanism to deliver “More than Moore” will come from integration of multiple circuit types through SoC and SiP technology.

SiP VERSUS SoC

The benefits of “More than Moore” can be realized through both SoC and SiP technology. Each approach has specific advantages and both will be used in the future.

The most important as the electronics industry becomes ever more dominated by the consumer will be System in Package. This will allow the efficient use of three dimensions through innovation in packaging and interconnect technology. The result will support continued increase in functional density and decrease in cost per function as the industry proceeds towards 14 nm and below. A comparison of SoC and SiP architectures is shown in Table HI-15. It should be noted that any SoC may be used as a component for a complex SiP product.

System in Package (SiP) technology is rapidly evolved from specialty technologies used in specific applications to a set of broad and high volume technologies with wide ranging impact on electronics markets. The rapidly evolving and adoption of SiP has been for stacked memory/logic devices such as in Packaging on {Package (POP) and Package in Package (PIP) in smart phone and tablet applications. Numerous variations of die stacking, package stacking, side by side packaging are being implemented driven largely by the demands of mobile consumer products. With the emergence of interposer technologies (silicon, organic, glass etc.) the field is wide open for innovations in SiP technologies to broaden the scope and realize the promise for More than Moore and

DEFINITION OF SiP

System in Package (SiP) is a combination of multiple active electronic components of different functionality, assembled in a single unit, which provides multiple functions associated with a system or sub-system. A SiP may optionally contain passives, MEMS, optical components, and other packages and devices

There are many types of SiP packages. They are divided into horizontal placement, stacked structures, and embedded structures. Examples of the major categories are shown in Figure 32.

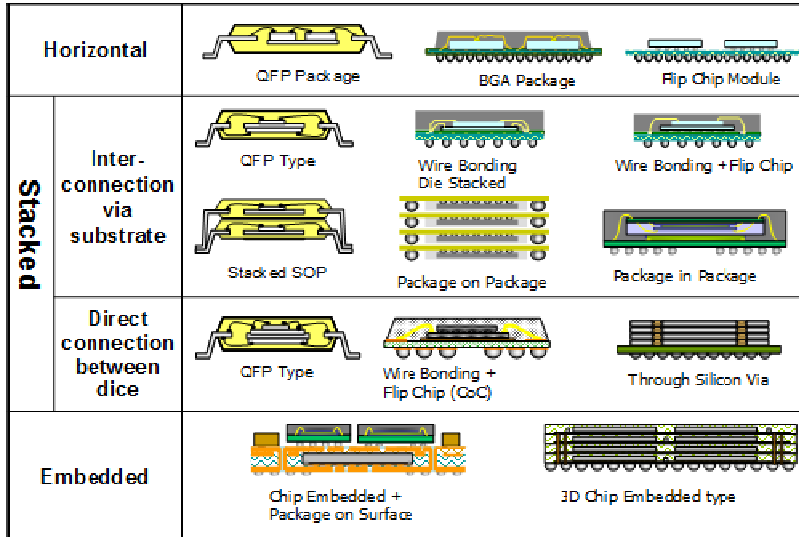


Figure 32: Categories of SiP

SIP IMPLEMENTATIONS AND PACKAGE ON PACKAGE

An example of combining packaging technologies is the hybrid (flip chip and wirebond) package stacking memory (flash, DDR, SRAM) die on top of an ASIC into one package, utilizing wirebond for the top die and flip chip for the bottom die, molded altogether utilizing the basic tools in the assembly and packaging engineers' tool box. With the advancements and in wirebond technology to Cu Wirebond and Flip Chip technology to Cu Pillar, hybrid packages were implemented in these technologies starting at the 28 nm technology node (Figure 33). These hybrid packages are being designed and implemented in mobile applications such as cell phones and consumer products such as digital cameras and camcorders are in use today. They are being rapidly replaced with hybrids using wafer level packaging, direct interconnect bonding and μ bump flip chip bonding further reducing size, power, latency and cost.



Figure 33: Hybrid package combining wire bond and flip chip for 3D SiP

Combining stacking and side-by-side multichip module BGAs are used across the PC, consumer and communication applications for their low cost, design flexibility and proven technology. Particularly important would be the integration of several different semiconductor technologies, from different foundries onto a single package.

Shown below is a Samsung 64 GB NAND memory (Figure 34). There are 16 NAND die staggered and stacked plus a controller die. The NAND die has been thinned to 25 μm with 10 μm die attach between die. This is an early example of multiplying density through 3D stacking while maintaining thickness and footprint.

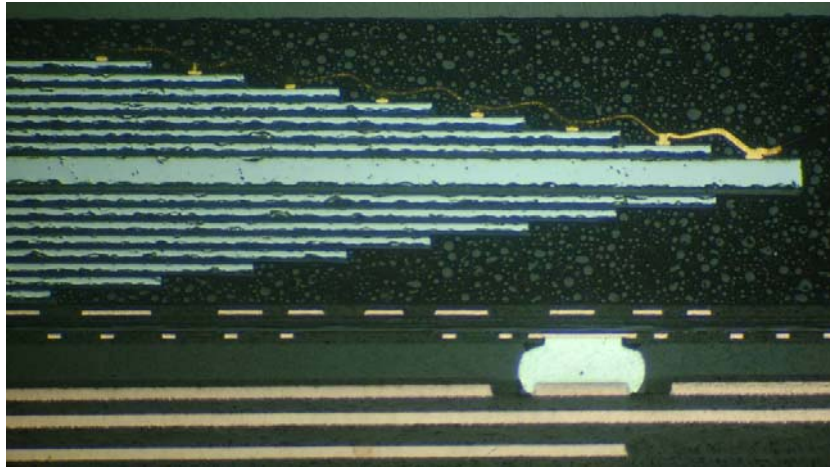


Figure 34: 3D staggered stacked NAND flash package with wire bond interconnect.

The state of the art today replaces the wire bond in the staggered die stack with stacked die using TSV interconnects between die. The specification for the device using the TSV based package has higher speed, decreased package volume, decreased latency and has reduced operating power 50% (Toshiba data). The specification for this SiP is in the table below.

Package Type		NAND Dual x8 BGA-152	
Storage Capacity (GB)		128	256
Number of Stacks		8	16
External Dimension (mm)	W	14	14
	D	18	18
	H	1.35	1.90
Interface		Toggle DDR	

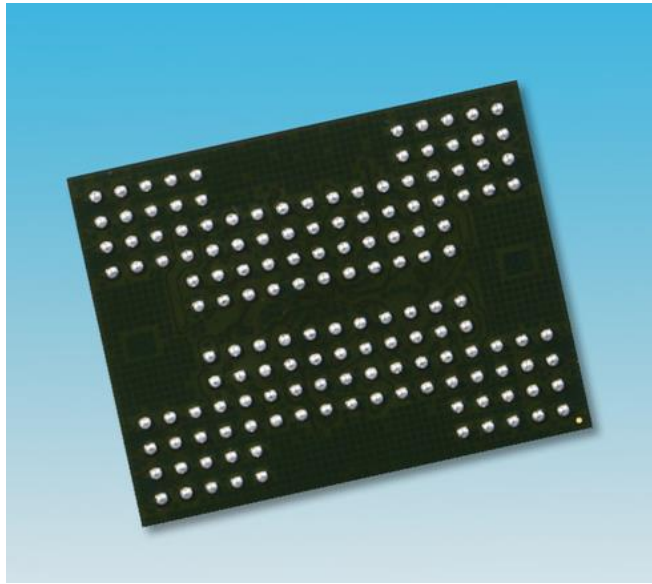


Figure 35: Bottom view of NAND stacked memory showing BGA solder balls

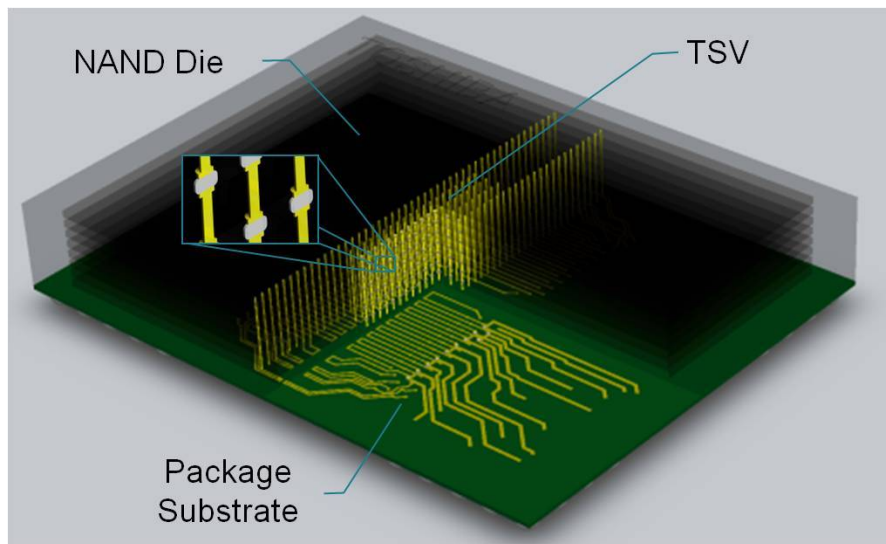


Figure 36: Illustration of TSV interconnect in the stacked die package

The initial SiP packages were memory and camera modules that are now manufactured in high volume. There were a limited number of circuit fabrics used. The emerging package types combine more function. . The package in figure 37 is 8.3 mm x 7.4 mm x 1.0 mm and it incorporates the functions of WLAN, Blue Tooth, GPS and FM and more into a single SiP. This package includes an SOC integrating WLAN and Blue Tooth on a single chip and an SiP integrating on package the SOC plus GPS and FM). This is an early example of SiP integrating multiple functions into a single miniaturized package.

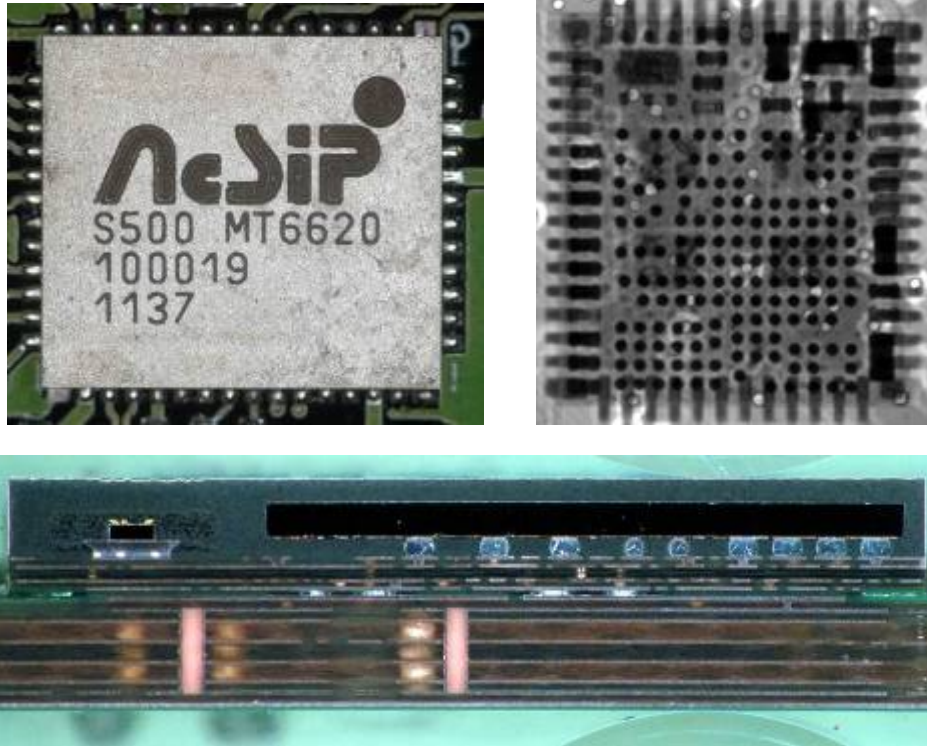


Figure 37: SiP incorporating SoC (WLAN & Blue Tooth) into SiP(SoC, GPS and FM)

PACKAGE-ON-PACKAGE (POP)

Package on Package (PoP) is perhaps the most important SIP package architecture today in the smart phone and tablet market (Figure 38). In this technology one package is placed on top of another while maintaining Z level interconnection.

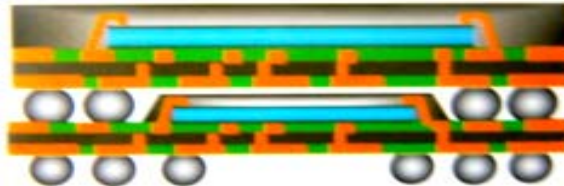


Figure 38: Package on Package (PoP) structure

The POP package designer usually uses the top package for memory application and the bottom package for processor, baseband or ASICs applications. The technical advantages are short distance connection between the processor and memory while maintaining the same small footprint. However, equally important, is that the top memory package is decoupled from the bottom processor, baseband or ASIC package for qualification, logistic handling, procurement and sourcing.

FUTURE COMPLEX 3D SiP

The SiP will continue to add complexity and to bring system level components closer together. The complex 3D SiP will incorporate both packages and components. An example of the coming level of integration is shown in figure 39.

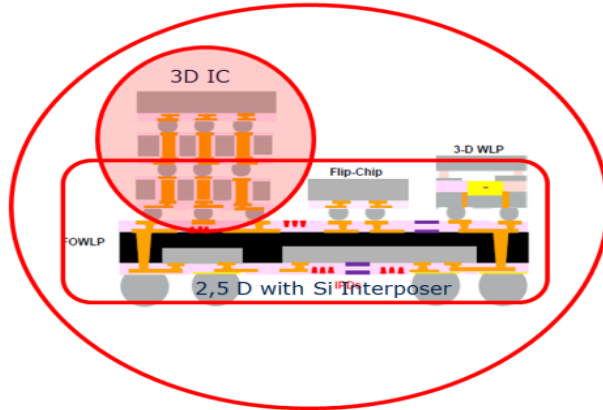


Figure 39: Example of Complex 3D-SiP using FOWLP, Interposer, 3D IC

Future designs will include digital, analog, logic, memory, MEMS, RF, photonics, passives and more in form factors that meet the requirements of specific applications. This will include the use of flex circuits, plasmonics and circuit/device types we have not yet conceived. An example of diversity by device type, materials and packaging technology is illustrated in figure 40 below.

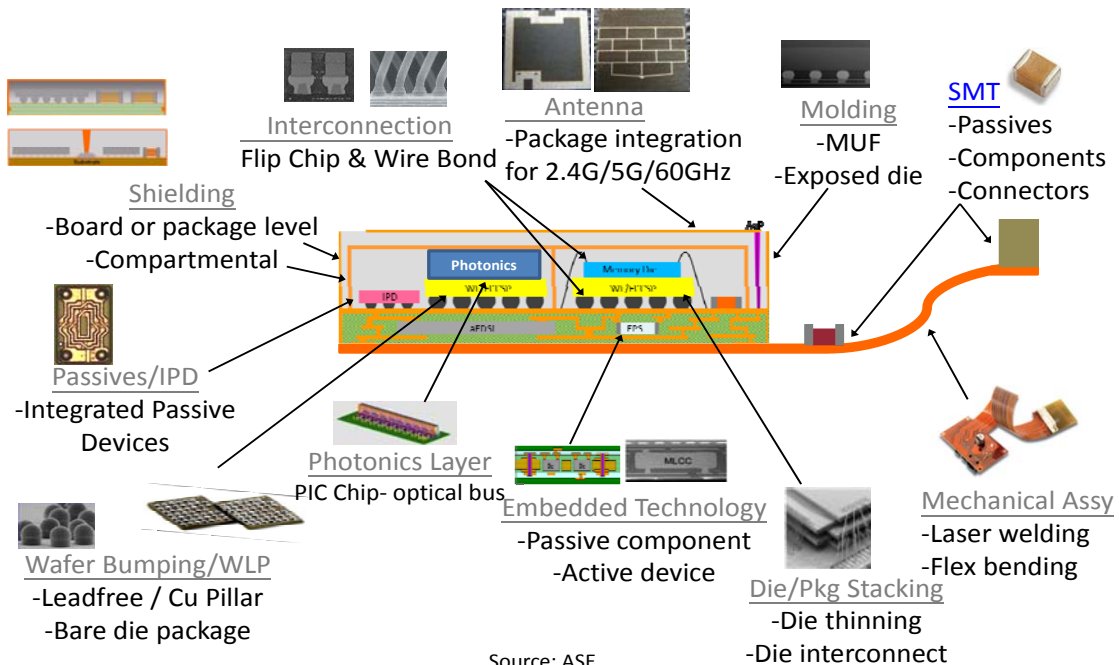


Figure 40: 3D SiP of the future illustrating available for application specific SiP

This structure cannot be realized commercially without new conductors and dielectrics that will be discussed in Section 13 of this Chapter.

SiP-LEVEL SYSTEM DESIGN VERSUS BOARD-LEVEL SYSTEM DESIGN

Besides the comparison with SoC, SiP is often compared with multiple monolithic packages for a new subsystem or system level product package. SiP has often been considered more costly than the corresponding combination of monolithic packages. It is sometimes true when only the packaging costs are compared. But the total cost of the system building and the accompanying advantages must be taken into account. SiP offers customers benefits of smaller footprint of devices and fewer numbers of connecting traces between devices, which results in lower number of PCB layers. Also shorter signal paths in SiP reduce electromagnetic emission and cross talk. These features were demonstrated by an experiment with the system composed of microprocessor and DDR memories (See Figure 41 below). Board-level system design was made of monolithic packages and built on a PCB, while SiP-level system design was embedded in SiP. Comparing with the board-level system design, the SiP-level system design reduced footprint by 80%, electromagnetic emission by -20 dB/μV and number of PCB layers from 6 to 4 layers.

These benefits can often offer SiP-level system design lower total cost in addition to the smaller size and higher quality of reduced noise and electromagnetic emission. Thus, the optimum system solution often can only be achieved by close collaboration and understanding between semiconductor/package/system suppliers.

SiP lightens a burden on designing a system board

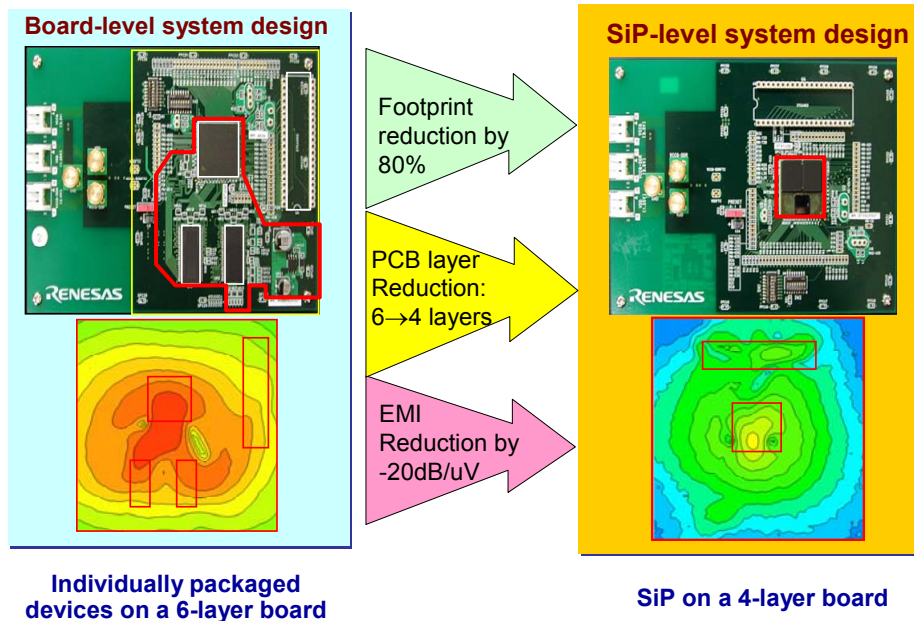


Figure 41: SiP design improves footprint, reduces PCB layers reduction and improves performance

DIFFICULT CHALLENGES FOR SiP

System integration is aimed at higher performance, miniaturization, heterogeneous integration, lower power requirement, lower latency and cost advantages at the package and system level. Many critical technology challenges must be solved to achieve the ultimate performance goals and other benefits of SiP. The difficult challenges for SiP are presented in Table HI-13.

THERMAL MANAGEMENT FOR SiP

Today we encounter hot spots in integrated circuits which have circuit elements of different thermal density in the same IC. This presents a problem for package design but it has known solutions (see further in this Chapter: Single chip packaging). The problem is becoming more difficult as the industry introduces new generations of microprocessors with many cores and incorporates core hopping to address local heating problems. These hot spot problems are exacerbated by the fact that we now have no way to know where the hot spot will be located since it will move during operation. Finally we may have circuits included in a SiP with different maximum junction temperature. The specific requirements to provide a cost effective mechanism to manage junction temperature while minimizing test time remains a major challenge for testing complex SiP devices.

All of the thermal management solutions discussed in Section 7 of this chapter may be applied to SiP, particularly when they involve the integration of 3D components.

THERMAL CHALLENGE OF HOT SPOTS IN SiP

The heat generation from an IC is highly non-uniform with areas of very high local heat fluxes at few locations on the die. Future trends show an increase in thermal design power and an increase in both average power density and local power density (also known as “hot spots”). Hot spot thermal management limits the thermal solution for the package. Even when total power of the component remains within design specification, the hot spot power density increase could limit the device performance and reliability.

For a SiP, thermal management must take account of the hot spot thermal dissipation within the die as well as within the package. Higher power dissipation with suboptimal placement of heat sources increases the risk of “hot spots” in 2D/3D integrated circuits. Also, removing heat from the interspersed chips with relatively poorly conducting thermal interfaces in 3D die stacking becomes very difficult (e.g. thermal impedance of C4 attach/underfill for flip-chip package, thermal resistance of chip attach material for low density wire-bond package) and it increases the cooling challenge of hot spots in SiP.

COOLING SOLUTION DESIGN REQUIREMENTS FOR SiP

For stacked die configuration and for embedded device configurations, the decreased volume and available exposed surface provide significant challenges. For low profile packages with 3D die stacking, various package and system level thermal solutions should be considered. The hot devices need to be located with due consideration for various primary heat flow paths as shown below in Figure 42.

Hot spot on top has a relative smaller heat resistance to top side; but in general the heat resistance chip-(chip-to-chip, etc.) and substrate-system (chassis) is in the range of one magnitude smaller than natural convection including heat path to the top). An opportunity to improve the heat path to the top with double side cooling and an applied heat sink on top will influence system design, system cost and potentially system reliability.

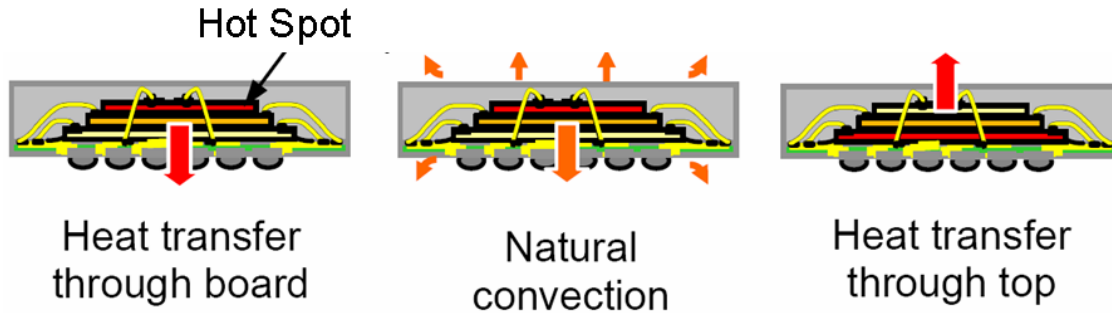


Figure 42: Location of High Power Die versus Primary Heat Flow Path

The hot spot generally occurs farthest from the primary surface used for heat dissipation. The higher power devices need to place closest to the primary heat-dissipating surface. Technology improvement to the primary heat flow paths needs to continue. For top side heat flow path, use of higher conductive molding compound, embedded heat spreaders and improved package to casing thermal interface material are potential thermal management options. For bottom side, i.e. board side, heat flow path, thermal performance enhancement options include use of thermally conductive under-fill between package and board, dummy solder balls between package and board, embedded heat spreader within the package substrate, and high conductive die attach between die and die to substrate. System level enhancement options include use of thermally conductive enclosure, venting grill, and active air moving thermal management device close to the device.

THERMAL CHALLENGES OF PROCESSOR AND MEMORY DIE STACKED SiP

In packaging a multichip module with one high power process and several low power memory chips, the preferred technique has been to locate the module lid precisely above the processor chip, permitting use of a thin layer of thermal interface material (TIM). The inevitable variations in chip heights and planarity of memory chips are accommodated by use of gap-pad (conductive elastomeric) TIM that results in significantly higher thermal resistance than that of the processor. Since the processor power density is typically several times that of the memory dice, resulting junction temperatures of all chips are similar.

For 3D stacked die configuration with TSV interconnects, the processor die is preferred to be placed at the bottom in 3D die stacking to make it closer to the substrate due to IO signal performance and power delivery efficiency, but cooling performance from the high power process will be the bottleneck. If the processor die is placed on the top, TSV requirements in both counts and size would cause significant mechanical concerns (e.g., crack, stress) for the memory dice at the bottom.

POWER DELIVERY/POWER INTEGRITY

The power level of high-end microprocessors places very stringent requirements on power integrity as the power density increases and the operating voltage decreases. The power integrity and product cost requirements cannot be met for high performance devices without chip/package/system co-design. (See section 9 on The Need for Co-Design and simulation tools) The voltage level for 22 nm and smaller node devices are in the sub one volt range resulting in reduced noise margin. Even with low resistive losses, the higher current transients due to multiple cores on a chip requires lower interconnect inductance with more decoupling capacitance as close as possible to the transistors. For multi-chip packages, placement of the various chips and decoupling capacitors is crucial and requires system level simulations. For 3D stacks new materials will also be needed with higher dielectric constant and lower leakage currents to deliver the high capacitance density in the stack required to ensure power integrity at low cost.

Power delivery for multi-chip packages is also getting complicated due to multiple power supplies for different types of circuits such as core, memory, back-biasing, etc. Due to the test and system requirements, noise margins for the various power supplies are also different. Managing multiple power supplies requires more layers in the package which may restrict the use of some package technologies.

The reduction of power at the system level and the need to minimize transient voltage excursions future Complex SiPs will require on package and perhaps even on chip power convertors/controllers. Delivery to the package may be 100V or more while the operating voltage for some devices will be below 300mV. Conversion efficiency of more than 96% has been achieved. In addition power control is needed to turn power on and off to circuits when they are temporarily not needed. Fast switching with very low inductance will be needed to ensure that inductive kick-back does not force voltage out of specification.

Reducing operating voltage dynamically depending on work load will also be enabled by local power controllers either on chip or on the package. All these techniques will be needed to reduce thermal density.

TESTING OF SiP

The complexity of SiP based products continues to increase and, with that, test becomes a more difficult problem. The testing is further complicated by the fact that at current and future CMOS nodes transistors will wear out. Known good die will not be sufficient to ensure a reliable system. The challenges are many and they include:

- test access
- contacting for testing thinned wafers and/or thinned die
- thermal management during test
- testing mechanical and thermal characteristics in addition to electrical test
- Continuous test while running, intelligent redundancy and dynamic self repair to ensure reliability

TEST ACCESS

If we assume that we begin the assembly and packaging process with known good die (KGD) the test problem is limited to confirming the assembly process and testing the performance of the on-package interconnect. If SiP is to meet its potential the off-chip drivers will be similar to the core transistors and only the off-package drivers will require more power. The SiP will not deliver all the test points to package pins for these more complex packages. There are several potential solutions including the incorporation of a “BIST” chip on-package that can have access to device pins that are not delivered to package pins.

CONTACTS

The continued reduction in contact pad geometries is approaching a terminal density that cannot be met with even the leading edge of conventional MEMS contactors. Several solutions are being evaluated including capacitive coupling which will suffice for digital signals but cannot provide power delivery or appropriate contact for analog signals. RF contactors have also been proposed and may offer a solution for some contact challenges. None of these proposed solutions has been proven to meet the requirements.

The test contactor required to deliver KGD for thinned wafers/die may be an even more difficult problem. The competition between ensuring power integrity when contacting these thinned dies and damage to the die associated with the contactor force and potential pad damage poses an ongoing challenge.

These challenges and others may prevent the industry from delivering KGD for thinned wafers as we approach devices with billions of transistors. The concept of “probably good die” with redundancy in the SiP is one approach for ensuring the quality (including reliability) of complex SiP products.

MECHANICAL AND THERMAL TESTING

The thermal cycles and specific use cases for many consumer products impose mechanical stresses that require test to ensure reliability of the products. The “drop test” approaches that have been used for cell phones and some other consumer products need to be replaced by new approaches that test a wider range of stresses including those associated with the thermal cycles experienced in the use cases. In addition we need tests that fit in a production flow without excessive test time or test cost. This remains a challenge not yet met.

COST OF TEST

These test challenges must be met with low cost. Most SiP are today are used in consumer electronics. These markets are very price sensitive and any SiP for the consumer market with excessive test cost will not be successful. The major elements of conventional test cost are applications programming, test time, cost of ATE equipment, and cost of probe cards. Complex SiPs may require both conventional test and BIST testing to accomplish adequate testing. This is due to test access limitations in high

component density, the very high speed of RF and digital communications circuits, and the requirement to test system level characteristics.

We have introduced some of the details for test challenges that are specifically relevant to assembly and packaging. The Test Chapter of the ITRS should be reviewed for a more complete description of test challenges.

DIFFICULT CHALLENGES FOR SiP

The major challenges for digital systems today are power requirement and integrity, thermal management and the limitations in physical density of bandwidth. These challenges become more difficult in 3D-TSV SiP architectures. In this section we will only address the packaging issues related to these challenges. Work aimed at reducing power requirements such as new transistor materials and development of new architectures to reduce leakage currents is addressed in other chapters of the Roadmap. Table HI-13 lists these challenges. The three most important defined above are addressed in the coming paragraphs.

POWER REQUIREMENTS AND INTEGRITY

The total power requirement can be reduced by dropping the operating voltage, reducing the interconnect distance, reducing the capacitance and reducing the operating frequency. Stacking the circuits in layers will reduce the interconnect length by approximately the square root of the number of layers. Today a majority of the power is associated with interconnects so stacking 4 layers may approach a reduction in power requirement by a factor of 2. This depends on the % of power in the metal 1 and metal 2 layers which is more than that of the global interconnect.

- The frequency capability of the logic transistors exceeds the frequency used so a reduction in operating voltage can be realized without compromise in performance. The power consumption is proportional to the square of the voltage so a reduction to half can reduce power requirement by four. This is very effective if the power integrity can ensure keeping the transistors above the voltage threshold.
- Reducing the frequency results in major reductions in power. Stacking the die enables a much larger number of cores and, to first order, an increase by an order of magnitude in the number of cores can deliver similar computing power when the frequency is reduced by an order of magnitude.
- Reducing the capacitance will require new material for interlayer dielectric. Today the state of the art is k_{eff} of about 2.6. Material currently in qualification can drop this number to below 2.0. This provides both a performance improvement and reduction of power required.

Power integrity is much more difficult when the voltage is near the low voltage threshold and the potential exists for billions of transistors to switch essentially simultaneously. When these transistors are stacked the inductance in the wiring between the power source and the transistors must be decoupled as close as possible to the transistors. The incorporation of interposers in the stack with capacitors of very high capacitance can

accomplish this task. This will also require new materials since the dielectric constant of approximately 4.0 used for on chip/on package capacitors today is too low to provide the required capacitance. New materials in qualification may increase this number to 100 or greater.

THERMAL MANAGEMENT

The thermal density is increased and the surface area to exhaust the heat is reduced with 3D integration. The steps defined above to reduce power requirements will help but the stacked die architectures for logic devices will require heat removal from inside the stack. The approaches to accomplish this are addressed earlier in this section.

PHYSICAL DENSITY OF BANDWIDTH

As the density and performance of the logic circuits are increased and the physical area available to address the resulting increase in demand for bandwidth is reduced new approaches are necessary. There have been proposals to bring photonic data transmission to the IC. These proposals may address the bandwidth but the wavelength employed for photonic data transmission is many times larger than the transistors. In addition, using an indirect band gap material requires more energy than a direct band gap material for converting data from electrical to optical and back.

The solution is to bring photonics to a direct bandgap semiconductor circuit in a SiP package and convert to a very wide electrical bus on the package. The photonic connection must use wavelength multiplexing in a single mode fiber to reach the physical density of bandwidth required for future SiPs.

9. THE NEED FOR COHERENT CHIP-PACKAGE-SYSTEM CO-DESIGN, MODELING AND SIMULATION

Issues include:

- Data exchange
- Materials properties
 - Mechanical
 - Chemical
 - Electrical
 - Thermal
 - Optical

OVERALL REQUIREMENTS

Chip-package-system co-design methodology is a vital enabler for integrating SoCs, other die, MEMS devices and passive components efficiently into System-in-Package.

Chip-package-board design collaboration is essential to reduce cycle time and cost and to optimize performance for stacked die, PoP, PiP, and 3D packaging in general. Failure to identify and meet essential system-level requirements and to apply lessons-learned, will result in lower-than-expected performance. Understanding design trade-offs and the performing critical system-level analysis is essential to produce designs that can meet the desired cost and performance targets. Incomplete feasibility studies and failure to capture key interactions at the system level can result in extra iterations before the package design is finalized. It is important to identify essential system-level requirements and to apply lessons-learned for good optimal design. Without the benefit of co-design and simulation, there is risk that a device will be late to market with an expensive, overly conservative package.

Some key challenges in 3D packaging are design for manufacturability, design for low cost, reducing design time, design for reliability, complex wire bond and/or flip chip rules checking, chip design flexibility trade-offs. Also critical is interface/alignment with tools and flows such as those provided by EDA design software tools, IDM specific design flow and tools, and alignment with substrate suppliers and assembly sites. Implementing co-design methodology requires iterative design reviews; collaboration between chip, package and system design; application development; electrical, thermal, and mechanical modeling; simulation, and high-density substrate design teams. A suggested design flow is shown in Figure 43 below.

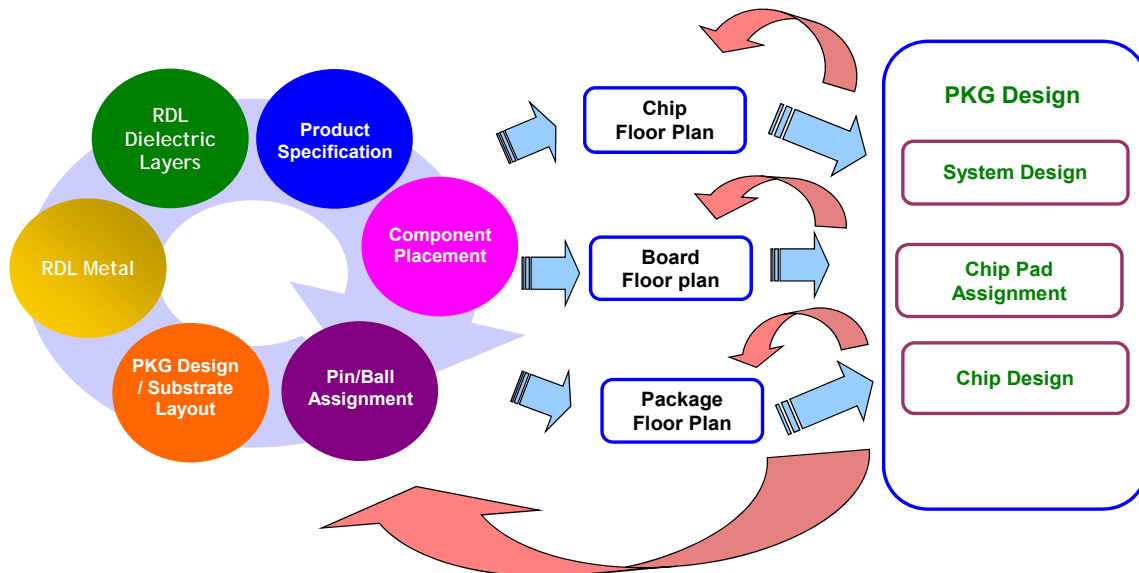


Figure43X: Chip-Package-System Co-Design Flow

The co-design, modeling and simulation issues are dealt with in more detail in other Chapters of the Roadmap.

CO-SIMULATION OF RF, ANALOG/MIXED SIGNAL, DSP, EM, AND DIGITAL

SiPs that combine RF, analog/mixed signal, DSP, and digital bring not only design and manufacturing challenges but also simulation challenges. Usually different functions of

an IC require a different simulation technology. For instance, frequency domain simulations such as Harmonic Balance are adequate simulation technologies for RF circuit designs; whereas time domain simulations are typically used to predict nonlinearity and VHDL or C based system simulation for digital applications. It is important to understand the system's behavior with packages and interconnect parasitics. Simulation and Modeling of Embedded Passives and Integrated Passive Devices in SiP applications need to be considered. Embedded passives are used to replace traditional surface mount parts. Cost and delay associated with optimizing a new device by design-fabrication-characterization-redesign-fabrication iterations will not be commercially viable. Design optimization must be done by simulation in the future and that simulation must contemplate all interactions in the design to delivery supply chain as illustrated in Figure 44.

Future Interaction Challenges

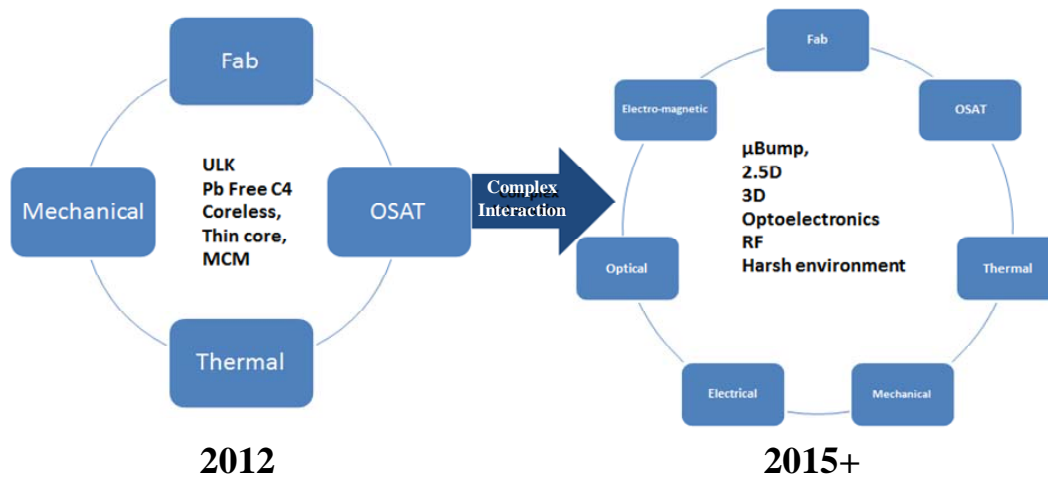


Figure 44: Challenges of interaction across technologies and the supply chain

COLLABORATION, COST AND TIME TO MARKET

Expert users of each tool for chip/package/system must collaborate to optimize the design. Thus, for the future, appropriate user interfaces are required. Co-design can improve performance while reducing costs and cycle time dramatically—often by 2X. Without the benefit of extraordinary collaboration within the design team, the package is almost impossible to optimize at the system level. The cost trade-offs would not be clear, system level performance impacts would be uncertain, and changes would be cumbersome or impossible to implement efficiently. To avoid this, designers often use overly conservative design margins and assumptions that lead to higher package costs.

DESIGN FOR RELIABILITY IN SiP

Effective co-design should comprehend the interaction between functional, physical, thermal, mechanical, electrical, chemical properties and reliability. Many of the trade-offs

between design areas and reliability that are evident in conventional packaging become more complex for SiP configurations. Thus, it is not practical, especially in SiPs, to run the electrical, mechanical, thermal and reliability design portions separately. Because of the complexity of sub-component interactions, there is no universal or specific list of parameters to design for reliability. In general, one needs to examine the sub-component interactions, design goals, trade-offs, design rules, specifications, and existing design for reliability practices in order to select the appropriate design for reliability guidelines.

GENERIC CHIP-PACKAGE-SYSTEM CO-DESIGN TOOL REQUIREMENTS

- Improve design cycle time, accuracy and design-for-manufacturability
- Align with critical tools, import/export data formats, flows and rules such as: IDM's internal tools die design tools, suppliers, assembly sites, electrical constraints and modeling tools
- Reduce iterations, less manual/more automated checking, capture complex design rules and enable more chip-package-system trade-off capabilities
- Forward-looking: better methods, more complexity, collaboration, and technology combinations
- Easier verification: Substrate, substrate plus die, manufacturability, electrical, functional, thermal, and mechanical verification. Import/export to IDMs internal tools
- Easier and more rapid feasibility analysis
- Collaboration with die and system design teams. Unified data formats, chip plus package plus system verification tools, etc.
- Comprehend the interaction and I/O planning of multiple functions within a single package (also passives)
- Great complexity—amount of design data, multiple layers, elaborate patterns, multiple net lists
- Complicated electrical constraints (long traces/wires, crossing traces/wires...). Enhanced constrain management
- Allow minor tweaks in IC or package design without leading to significant cycle time hit
- Need faster design iterations in early phase to avoid more costly design iterations in the later phase
- Capture complex mechanical, wire bond and flip chip bond assembly-rule constraints driven by smaller and thinner packages
- Better design for manufacturability and cost analysis. More and easier to use manufacturability constraints
- Real-time chip-package-system design trade-offs
- Interface and alignment with internal tools and flows
- Shortening design cycle of complex designs
- Cost-weighting of constraints
- More flexibility to handle frequent design changes
- Flexibility of design flow, user-defined design starting point from chip or from system

- Tighter integration with chip, system and manufacturability design teams
- System-level electrical modeling, including high-speed applications
- Complexity drives verification tools that work across different design environments
- Tight collaboration with suppliers, support, development, production, and customers to enable better methods and tools for complex package co-design
- More powerful user-friendly scripting capabilities
- Common, technology independent database to enable reuse

10. PACKAGING FOR SPECIALIZED FUNCTIONS

TECHNICAL CHALLENGES

The new technologies that are becoming available must meet the challenges of the previous section – bandwidth, power, thermal and environmental.

The packaging technology that will be developed and integrated into high-end systems will be those that are developed with acceptable cost and performance.

TSV

Through Silicon Vias enabling 2.5D silicon interposers and 3D chip stacking providing high-density interconnect and, therefore, high bandwidth capability between components. Also glass interposers may be a factor for some applications with Through Glass Vias (TGV) providing advanced connectivity. Memory modules are already introduced and applications will expand.

ADVANCED PACKAGING -- SIP AND POP

Systems in Package and Package on Package technologies provide the capability of optimizing cost and function in a package. Integrating voltage regulation and silicon photonics with processor chips or bridge chips will be increasing. The mobile systems are where the current growth driver in this technology segment originates. However, the high-end systems will adopt these advanced package technologies because the increased interconnect pins, more memory, and more cores when placed in close proximity enables high-bandwidth interconnect in the existing power envelope. These tradeoffs will make the appropriate technology aspects economically scalable from mobile to high-end systems.

OPTICS

Optical interconnect will continue to be used more broadly. First, transceivers and active optical cables (AOC) will be used more broadly for in-frame communication, potentially replacing copper interconnect in backplanes or cables when the cost, power and bandwidth tradeoffs justify the switch to optical. Integrating optical devices into packaging to reduce trace length and, thus, power demand for high bandwidth interfaces

will demand advanced packaging and leverage the SiP and PoP technology components for increasing integration at the package level.

ELECTRICAL CONNECTORS FOR PACKAGES AND CARDS

Electrical interconnection will continue to be the dominant interconnection for short reach communication. The developing signaling standards are in discussion to go beyond 50 Gb/s per channel. Electrical connectors for printed circuit board and cable communication delivering low insertion loss, flat impedance profiles and minimal crosstalk will maximize the reach of the copper interconnect at an acceptable bit error rate. The speed of adoption of the higher speeds will depend on the ability to equalize the channels in the existing power envelop while the channel cost-performance as measured in \$/Gb/s is reduced over time. The cost-performance is strongly impacted by bandwidth density. Bandwidth density can be channels x Gb/s/channel per unit area for a package on a printed circuit board or channels x Gb/s/channel per unit length for card edge interconnection. The required ground pins that provide shielding of signals and a continuous return path will increase the effective number of pins per channel. So even in cases where the channels per unit area or channels per unit length are constant, the number of pins may increase to effectively shield the signals.

LOW-LOSS ELECTRICAL FOR PACKAGES AND CARDS

Reduced dielectric loss materials are increasing used for the high-speed electrical channels and the demand for those materials will increase as speeds above 50 Gb/s/channel are adopted. However, low-loss electrical also requires attention to processing and design of all the elements of packages and printed circuit boards. The copper roughness, via stubs, antipad size and shape, and internal via and PTH design are all as important as the loss characteristics of the dielectric material. Coreless packages and thin laminates for improved via and PTH design will reduce discontinuities significantly for high-speed channels. The footprint design at the electrical connector will require special design to avoid becoming the bandwidth limiting factor in a package to board, backplane or cable interconnection. This footprint design includes, via or PTH diameter, length and stub, antipad size and shape routing escape from the via or PTH and land sizes. Reference plane gaps, holes and interconnection to PTHs that create return path discontinuities are part of the channel design.

EFFICIENT POWER DISTRIBUTION

To efficiently address these technology challenges, the power efficiency must also continue to improve. The channel shielding requirements demands a greater amount of layers and vias for the high-speed channel while improving the power efficiency demands lower impedance power distribution for less loss through I^2R loss and less inductance for faster regulation. This creates a trend towards more metal and placing regulation closer to the loads competing with the short reach signaling and increased signal shielding. These trends also leverage the advanced packaging concepts of TSV and SiP and PoP described above and is part of the economic driver to adopt this technology.

OPTOELECTRONIC PACKAGING

SCOPE

This section covers semiconductor-packaging topics related to the use of photons to transmit data over distances of 100s of km down to mm on-chip. It also covers the packaging challenges associated with both photonic integrated circuits and the Heterogeneous integration of those components into complex 3D-SiP systems.

There are a large number of devices that involve photons that share the common requirement of providing a photon path either into or out of the package or both. They include:

1. Light emitting diodes (LEDs)
2. Laser diodes
3. Plasmonic photon emitters
4. Photonic Integrated circuits (PICs)
5. MEMS optical switching devices
6. Camera modules
7. Optical modulators
8. Active optical cables
9. E to O and O to E converters
10. Optical sensors (photo diodes and other types)
11. WDM multiplexers and de-multiplexers

These devices have widely varying packaging requirements in power, photon access, alignment accuracy, stress management, thermal control etc. that can be handled addressed in a single component package but become much more challenging when they are integrated into a 3D-Heterogeneous SiP package. The difficult challenges associated with optical packaging are listed in table HI-21.

PHOTONIC SENSORS

Photonic sensors are a special case since they do not transmit data but instead they create it. There are a number of important photonic sensor types with a variety of application such as harsh environments, military and biomedical applications some of which are included in Figure 45.

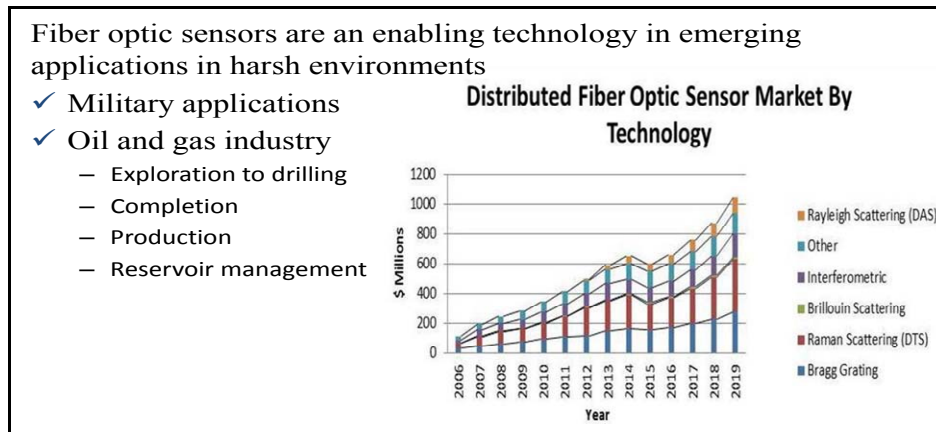


Figure 54: Photonic sensors for different applications

Research and development for optical sensors is progressing rapidly with 4 categories of sensors listed below that have different packaging requirements.

1. **Spectroscopy based**
2. **Capture based (functionalized capture surfaces or volumes)**
3. **Gas based detection (atmospheric and other gases)**
4. **Liquid based**

The R&D systems in use today are still in the bench top prototype phase as shown in Figure 55.

Integration of microfluidics and temperature control

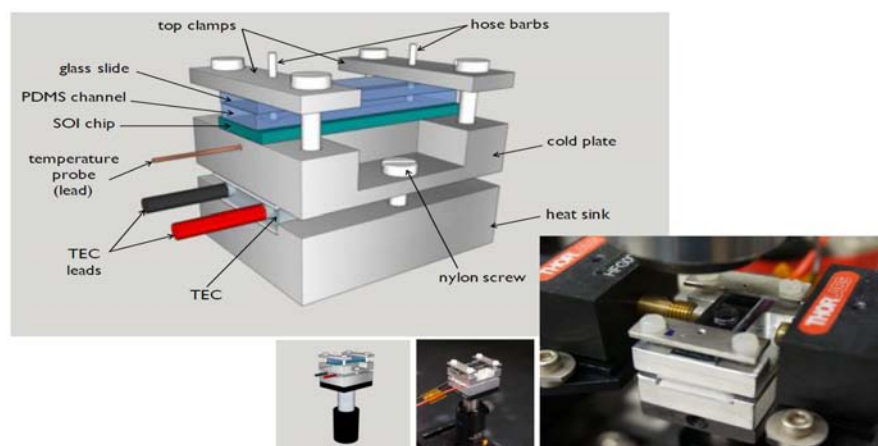


Figure 55: Fluidics sensor with temperature control used in R&D today¹

¹ Making good on our promises: Optical sensing from the lab to the real world Benjamin L. Miller, Departments of Dermatology, Biochemistry and Biophysics, and Biomedical Engineering, University of Rochester

This technology can be converted into a PIC chip using the processing techniques used in manufacturing of MEMS devices today. The challenge will be with the photonic connection to the package and the fluid connection to the sample source with the cost and reliability required in the application. The most probably solution for the photon source is to fabricate the lasers needed on the PIC chip as illustrated in Figure 56.

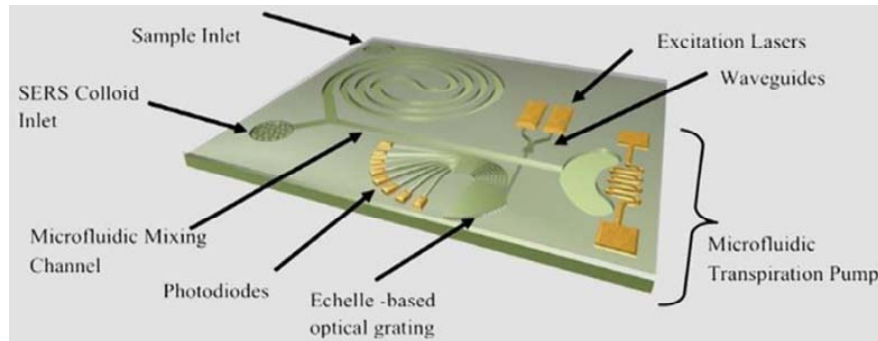


Figure 56: Photonic microfluidic based sensor on a PIC chip with no off chip optical connection

OPTICAL DATA TRANSMISSION

Long distance data transmission has been dominated by WDM single mode photonic signaling since the 1990s providing high density, low energy data bandwidth not available from any other technology. The packaging for this application is now well known and the unit volume is low in comparison to other applications such as optical data transmission in a modern datacenter. The solutions for photonics packaging in this application are not projected to change rapidly and will not be addressed in detail in this Chapter. There are now a large number of optical packages that are in production illustrated in figure HI-20 showing the wide range of package types and the adoption of packaging technology from electronic IC packaging.

SILICON PHOTONICS

The desire for higher level of integration for optical signals is driving the adoption of silicon photonics. The complexity of the challenge is increasing due to unique demands of heterogeneous integration of electronic/photonic circuits. This includes integration of diverse materials and diverse circuit fabric types into a single SiP architecture and the use of the 3rd dimension. Many of the problems are the same as those addressed in the on-chip difficult challenges section. The additional difficult challenges associated with the package are listed below.

1. **TSV Formation [Cost: Design, Process, Materials]** Aspect ratio (via last) drives cost higher and the differential CTE causes local stress.
2. **TSV Operation [Reliability: Design, Materials]** “Cu pumping” out of the vias on thermal cycling. Thinner layers and reduced CTE differential will be needed.
3. **TSV Keep out area [Design, Materials, Process]** Circuit density and cost are impacted large keep out area due to differential CTE and increased stress

sensitivity for photonic components. New materials and lower processing temperature are needed.

4. **Physical Density of Bandwidth [Size, Bandwidth: Design, Process, Materials]** Single mode WDM replacing multi-mode fiber/wave guides and integrated photonics chip supporting this capability on-package are needed.
5. **Low cost reliable optical connection to the package [Design, Materials equipment and Processes]** Process, materials and equipment for alignment/placement, bonding process for “wave guide soldering” to make cost effective and reliable connections to the package are needed.
6. **Low Cost Electronic/Photonic Package Substrate [Bandwidth, Waveguides, Design, Process, Materials]** Mechanical stability, thermal management, warpage control, photonic connections, electrical connections, integrated passive devices and other components will need to be accommodated. There are many candidates for package substrate material that satisfy some of the requirements including glass, silicon, organic and ceramic but none of them satisfy all requirements. Silicon has the advantages of good CTE match, high electrical bandwidth, compatibility with optical wave guides and the wealth of experience, equipment and process technology from silicon IC fabrication that can be cost effectively reused. Glass has many electrical advantages but has poor thermal conductivity. Organics lack mechanical stability. Ceramics are expensive and also have thermal management limitations. It is likely that more than one of these substrates will be used for different applications.
7. **Thinned Wafers/Die at Low Cost [Design, Equipment, Materials, Process]** Today thinned die are typically processed to 50 μ thickness and at that thickness will be warped to a level that they cannot be stacked without a method for maintaining flatness. Low cost residue adhesive and equipment to use it effectively in the thinning process will be required. Wafers in production will be thinned to 20 μ thickness and lower during the life of this Roadmap. Techniques that work are known today but are not cost effective.
8. **3D Stacking [Cost, Process, Bonding, Thermal Management]** The processes used today are complex can be simplified with some expensive steps removed to lower cost and improve reliability. New materials and designs will be required for thermal management. Low temperature processing will be required.
9. **Stacking Heterogeneous Components [Design, materials, process]** There may be applications where the lowest cost and highest performance will require stacking of Si circuits and compound semiconductor circuits in the same stack. Differences in stress sensitivity and mechanical/thermal properties. New designs and materials will be needed.

- 10. Noise and Cross Talk in SiP [Design, Process, Materials]** The SiP products will contain RF and other components that have low energy signals and logic that can draw high currents and impact the delivered power. Similarly as we reduce the physical separation of components in 3 dimensions cross talk can prevent proper operation. Some of these problems will become increasingly difficult as we reduce operating voltage due to both smaller geometries and the desire to reduce CV^2 energy requirements of the package. Designs that use optical signals where practical and shielding where optics is not practical will be required. New materials and processes will be required to manufacture these elements at low cost.

PACKAGE TEST DIFFICULT CHALLENGES

- 1. Known Good Die [Design, Test Contacts, Materials, Process, Equipment]** The packaging of multiple die in the same package has relied upon known good die to ensure yield after assembly. This will not ensure reliability when transistors wear out and VLSI ICs today do not produce known good die. When there are billions of transistors per IC and the geometries are measured in nano-meters all die will have some defects. Intelligently designed redundancy can ensure a high yield of functioning die as they have in memory circuits for years. The concepts and implementation of testing to ensure functioning die for logic is still a work in process. Contactless methods for test point access are being investigated but are not yet practical.
- 2. Testing Silicon Photonics Chips at Wafer/Panel Level [Design, Equipment, Materials]** Low cost production of Si Photonics will require manufacturing and testing of packages with a high degree of parallelism. Wafer level packaging will require testing at wafer level to maintain cost. The design of low cost test solutions for single mode WDM photonics will be required. These solutions will be dependent on the co-design of the Si photonics chip, the test point contact and the test equipment itself.
- 3. Low Cost Optical Test Access [Design, Materials, Process]** The incorporation of WDM single mode photonic signals on a package will require the ability to test the connections after package assembly. New concepts are under consideration but a cost effective solution does not exist. There will be design, materials and process changes to provide solutions.
- 4. 3D Stacking [Design, Testing, Testing Access Process, Equipment]** Testing and test access will require new designs for test access of stacked components. New test equipment to cost effectively test logic, memory, analog component, RF and passive devices in a single package will be required.
- 5. Test Contactors for Contact Pads Below 5 Microns Diameter [New Contact Methods, New Materials, Design]** The test contactors in use today for electronics damage the pads they contact. This problem will be exacerbated as test pads are driven to thinner metal and sub-micron geometries. New test methods, new contact methods and new access design will be required, all must be low cost.

6. **SiP Reliability [Design, Testing, Thermal Management]** The more difficult challenges are associated with testing in a world where transistors wear out. We will have no known good die, traditional test access points will not exist and thermal management when areal thermal density is increased by a multiple determined by the number of layers in a stack will all require solutions . Innovation in design, materials and test strategy will be required to meet these challenges. New processes and materials will be needed with built in self-test, continuous test while running, intelligent redundancy and dynamic self-repair will be part of the solution. New materials and modifications to equipment will be required.
7. **Ensuring System Reliability for Electronic/Photonic SiP based Systems [Design, Software, Fault Localization]** The potential for a single point fault to prevent operation of data communication and analysis systems does not meet market requirements. There are two paths to reduce this probability of a system level shut down due to a single point failure. One is the use of intelligent redundancy which is identified above. The second is a system capable of quickly obtaining the physical location of a fault during the product qualification process so that revisions can be made to the design to remove or reduce the weak points in the system. The design of such capability for individual integrated circuits has been explored for several years. Extending this capability to cover all components in a complex 3D Heterogeneous SiP is a very large task but will become a requirement to contain the cost of excess redundancy in these systems.
8. **Enabling the Software Defined Networks with Real Time Testing [Design, Software]** The diverse needs of users connected to the global network for access to the cloud will require SDN capability. This will not be practical unless the network hardware and software are configured to enable SDNs. This enablement will require low latency switching to set up the network and test capability to ensure that it is functioning correctly when set up and reliable during operation. The test challenge will require test resources at various points in the network that involve SiP incorporating FPGA technology.

DIFFICULT PACKAGING CHALLENGES BY CIRCUIT FABRIC

1. **Logic:** Hot spot locations not predictable, high thermal density, high frequency, unpredictable workload, limited by data bandwidth and data bottle-necks. High bandwidth data access will require new solutions to physical density of bandwidth.
2. **Memory:** Thermal density depends on memory type and thermal density differences drive changes in package architecture and materials, thinned device fault models, test & redundancy repair techniques. Packaging must support low latency, high bandwidth large (>1Tb) memory in a hierarchical architecture in a single package and/or SiP). Memory will have multiple circuit fabric types for various applications and each will have differences in packaging challenges.

3. **MEMS:** There is a virtually unlimited set of requirements; hermetic, non-hermetic, variable functional density, plumbing, stress control, and cost effective test solutions.
4. **Photonics:** Extreme sensitivity to thermal changes, O to E and E to O, Optical signal connections, new materials, new assembly techniques, new alignment and test techniques
5. **Plasmonics:** Requirements are yet to be determined but they will be different from other circuit types
6. **Micro-fluidics:** Sealing, thermal management and flow control must be incorporated into the package.

Most if not all of these will require new materials, new processes and new equipment for package assembly and test to meet the 15 year Roadmap requirements for electronic/photonic systems.

PACKAGING FOR MEMS

Micro Electro Mechanical Systems (MEMS) began to appear in the 1970s, initially for pressure sensors. Through the 1980's and 1990's there were many processes developed and a wide variety of MEMS devices including pressure sensors, microphones, accelerometers, ink jet printers, and eventually bio-MEMS devices. (see Heterogeneous Components Chapter) MEMS devices are packaged in an unusually wide variety of ways due to the great variation in requirements. These requirements, and the resulting package solutions, go well beyond those of microelectronic packaging and result in an unusual variety of packages.

Examples include MEMS packages for the following:

- Devices, such as transmit/receive switches, must exclude moisture to prevent deterioration or corrosion and might require an inert atmosphere to remain stable
- Pressure sensors must be open to atmospheric pressure but not be susceptible to moisture damage
- Optical devices, such as camera modules, must exclude particles, must not have organics that can condense on optical surfaces over time, require optical windows and must maintain optical chain alignment over the product life.
- Devices requiring controlled atmosphere; vacuum, inert gas, etc.
- Devices that analyze fluids require containment of those liquids and must not leak
- Devices requiring ESD protection greater than that required by CMOS devices

The commercial success of many of MEMS devices was limited by the lack of robust packaging technology. Initially, the typical approach to MEMS packaging was to use the technologies that had been developed for integrated circuits and other electronic devices. This ignored the critical differences between these MEMS devices and solid state

electronics resulting in packaging solutions that were not reliable and not suitable for the many use case environments such as automotive and consumer electronics.

One key technology used to reduce cost and improve performance of MEMS devices is the integration of MEMS with standard semiconductor devices that provide drive, control, and signal processing functions in a single package. This approach enables increased integration and reduction in cost. This may be enabled for many MEMS device types through a low cost wafer level package that can provide cavities. Technologies which enable the decoupling of package stress through the bump or die attach to the MEMS structure are also a critical challenge for MEMS in wafer level packages.

The approach consisting to introduce the cap at the wafer level (called Wafer Level Caps) is today in production. This technique requires further steps (wire bonding, over-molding, BGA). WLC caps are done for absolute pressure sensors, inertial sensors or capacitive sensors. Thin film encapsulation at the wafer level scale could be employed for RF MEMS and inertial MEMS (no contact with environment, specific pressure on cavity). Bonding technologies are developed with intermediate layer (glass frit, adhesive, metal) or without intermediate layer (anodic, direct or fusion bonding). The main technical challenge on WLC is to shift high vacuum and hermetic packaging for resonators and accelerometers sensors in order to increase the sensibility.

Wafer level packaging approach where the wafer encapsulation is doing with interconnections and bumps. The developments for WLP MEMS focus on developing capping technologies with through silicon vias, redistributive die layers and bumping steps. It's clearly the way to the 3D integration. Wafer level packaging is in volume production for inertial MEMS and Si microphones.

These differences that presented difficult challenges for packaging included:

- Mechanical fragility of the unpackaged devices
- Stress management, particularly for sensors
- Access to the environment outside the package (microphones, pressure sensors, microfluidics, etc.)
 - Acoustical signals
 - Light input for sensors and light output for digital light processing
 - Liquids (printers and pressure sensors)
- Protection of package contents from
 - Mechanical shock
 - Vibration
 - Electromagnetic interference
 - Chemically harsh environments
 - Light reaching the interior of the package
- Thermal management, particularly in SiP packages with component
 - “hot spots”

Several MEMS devices are now manufactured in volume and the packaging requirements are the limiting cost factor for most of them. Packaging costs account for between 50 and 80% of the cost of typical MEMS devices. The Roadmap does not yet address MEMS packaging in detail and there are no tables addressing MEMS packaging requirements in this Roadmap.

SEMICONDUCTOR PACKAGING FOR AUTOMOTIVE APPLICATIONS

AUTOMOTIVE ELECTRONICS

The rapid adoption of all electric vehicles and the coming introduction of self-driving vehicles is demanding rapid changes in automotive electronics with innovation required in essentially every portion of the vehicle. Internal networks are moving to photonics for weight and security, external networks must meet higher reliability standards, hundreds of sensors and tens of logic devices must be integrated and several must be monitored at millisecond time intervals. The roadmap for automotive electronics is also heavily impacted by regulation. The key parameters for automotive electronics are listed in Table HC-25 and the operating environment specification is in Table HI-26. These tables do not address the internal and external networks since the regulations are still a work in process but they will be added in 2016.

The table showing the roadmap for Automotive Electronics (Figure 57) is only defined through 2020 at this time due to the high rate of change and the unpredictable impact of government regulations that are needed for the self-driving vehicles. The energy density, regeneration efficiency, vehicle weight and charging rate will all be impacted and have a significant impact on the packaging requirements. The challenge will be to make the packaging technology a solution to some of the difficult challenges rather than the cause. The Roadmap will be expanded to address these issues in the next edition.

Roadmap of Automotive Electronics

Category	Characteristics	2016	2018	2020
Mileage	Medium car at JC08 mode	17	17.5	18
Power device	Inverter power density	16	23	30
	Specific on-resistance at breakdown voltage of 1.2kV	4 SiC/GaN	3 SiC/GaN	3 SiC/GaN
	Drain current density	500	500	600
	Die size Si SiC/GaN	169 49	196 64	196 81
Battery for HEV (high power)	Energy density	110	120	130
	Power density	4.2	4.4	4.5
Battery for BEV (High energy)	Energy density	230	240	250
	Power density	1.4	1.45	1.5
Capacitor	Capacity of capacitor pack	234	247	260
Motor	power	62	62	62
Network	Power train, body (CAN → FlexRay)	10	10	10
	Media, information	220	240	262
Sensor	Number of sensors	138	146	150
ECU	Number of ECUs	130	110	100

Figure 57: road map for automotive electronics

PACKAGING TECHNOLOGY DEVELOPMENT

From the roadmap of automotive electronics, the requirements for semiconductor packages are elicited for each part (See Figure 58 below). Main requirements include small footprint, high-temperature durability, low electrical resistivity, low thermal resistivity, effective cooling system, EM immunity, higher data rate, and system integration of sensors, processors and actuators.

Category	Trend	Requirements to packages
Power train - Combustion	<ul style="list-style-type: none"> •ECU-built in engine •Fuel-saving vehicle management 	<ul style="list-style-type: none"> •High-temperature durable packaging
Power train -Motor	<ul style="list-style-type: none"> •High power, fast switching devices •Intelligent battery management: 	<ul style="list-style-type: none"> •Lower Ron •Low Rth, cooling system •Management chip built-in cell
Network	<ul style="list-style-type: none"> •X-by-wire; FlexRay (10Mbps) •Longer harness (50km now) •Reducing number of MCUs by networking •Plastic optical fiber 	<ul style="list-style-type: none"> •Integration with network chip •Low impedance •EM immunity design •Higher-pin count packages •Smaller, cheaper EO devices
Information/ entertainment	<ul style="list-style-type: none"> •Probe-car infrastructure •Traffic information infrastructure 	<ul style="list-style-type: none"> •Higher data rate •Multiple communication path to outside sources
Body and security	<ul style="list-style-type: none"> •Integration of MEMS sensor, actuator, interface chip, etc. 	<ul style="list-style-type: none"> •Inverter-embedded motor •Integration
Safety	<ul style="list-style-type: none"> •Sensors and real-time processing •Monitoring a driver and lanes •Man-machine interface to inform the risk to the driver •Predictive safety mechanism 	<ul style="list-style-type: none"> •module self-generating electricity •High speed package •mm-wave devices •Sensor/CPU/actuator integrated module

Figure 58: Packaging requirements by category for automotive electronics

11. ADVANCED PACKAGING PROCESSES

SCOPE

The consumer driven market demand for products that are smaller, higher performance, lighter weight and have lower power requirements cannot be met without new materials and processes for packaging the devices used in these products. The innovations in processing include embedded devices (both active and passive), through silicon vias, wafer thinning as well as new methods of attaching the components of the package and the package contents to each other. This section addresses some of the most important of these emerging packaging processes.

EMBEDDED AND INTEGRATED PASSIVE AND ACTIVE DEVICES

The embedding of devices reduces footprint and decreases the distance between active and passive devices improving signal to noise ratio.

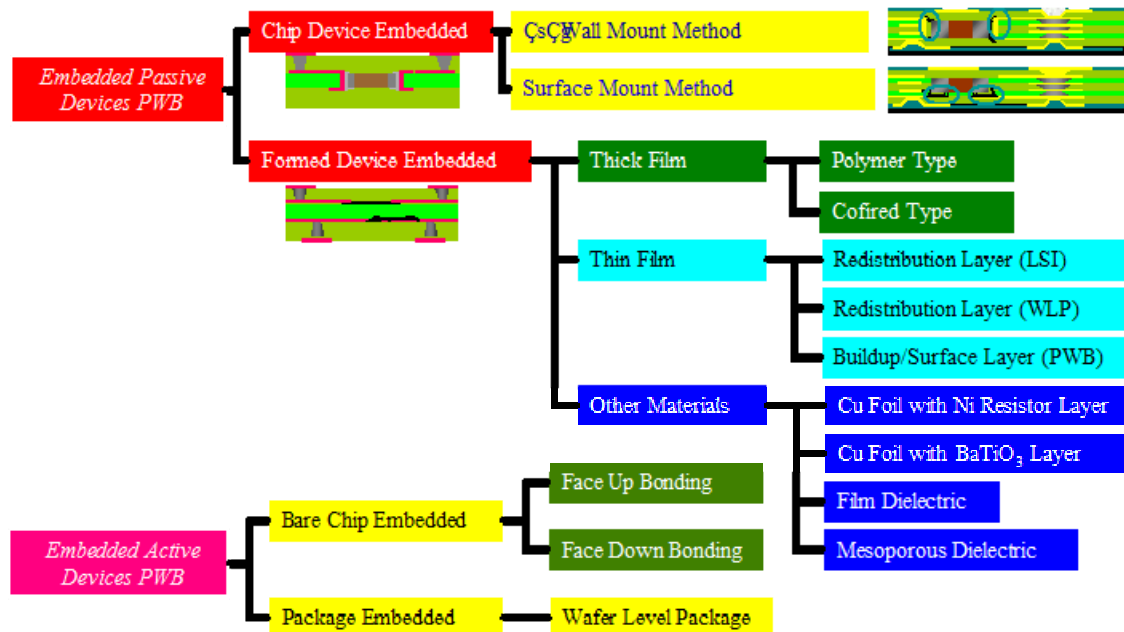


Figure 59: Overview of Embedded Passive Devices and Active Devices

The embedding of both active and passive devices is becoming a common practice (Figure 59). As SiP architecture continues to shrink system level products there will be increased use of embedded devices with logic, memory, passive devices as well as MEMS and sensors embedding in the package (including WLP), the package substrate and the printed circuit board. The challenges that must be overcome include:

1. Thermal management

2. Stress due to temperature differences and differential CTE between component and matrix
3. Test access

EMBEDDED PASSIVE DEVICES

The shrinking of memory and logic circuits and development of 3D and SiP packages has stimulated the need to reduce size of passive devices. For many years now resistors, capacitors and inductors have been fabricated using standard semiconductor processes. More recently integrated passive devices (IPDs) have emerged taking advantage of the benefits of transistor processing to increase density and reduce the size of passive devices. An example of an integrated passive device is shown in Figure 60.

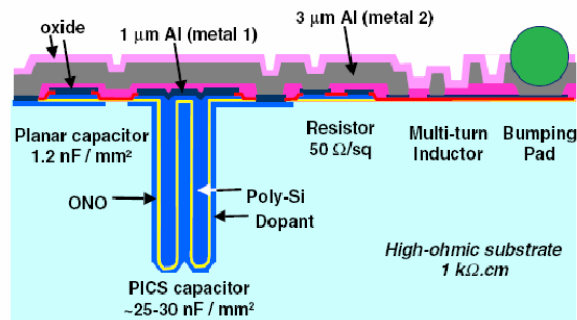


Figure 60: IPD with High Density “Trench” MOS Capacitors, Planar MIM, Multi-Turn Inductors, and Poly-Si Resistors

Examples of IPDs in production today are shown in Figure 61. These devices reduce the area required for these RF circuit components by up to 80% from the conventional SMD components.

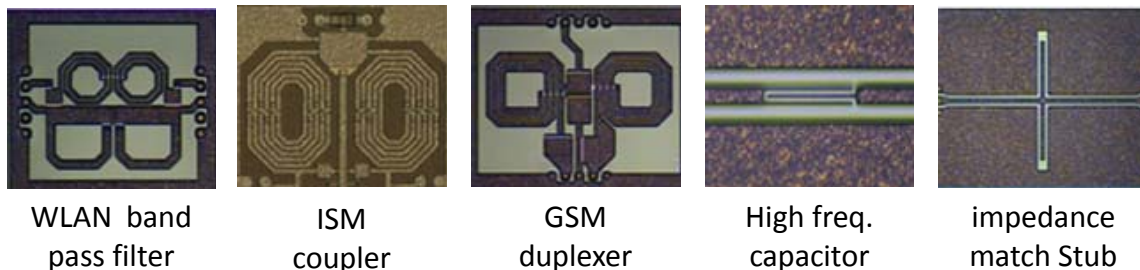


Figure 61: IPDs for RF packages

These devices may be integrated into a package as a circuit component or embedded into a circuit board or a package substrate providing reduced space, reduced interconnect complexity, improved tolerances with greater yield and improved reliability. Examples of how these devices are integrated into system are illustrated in figure 62.

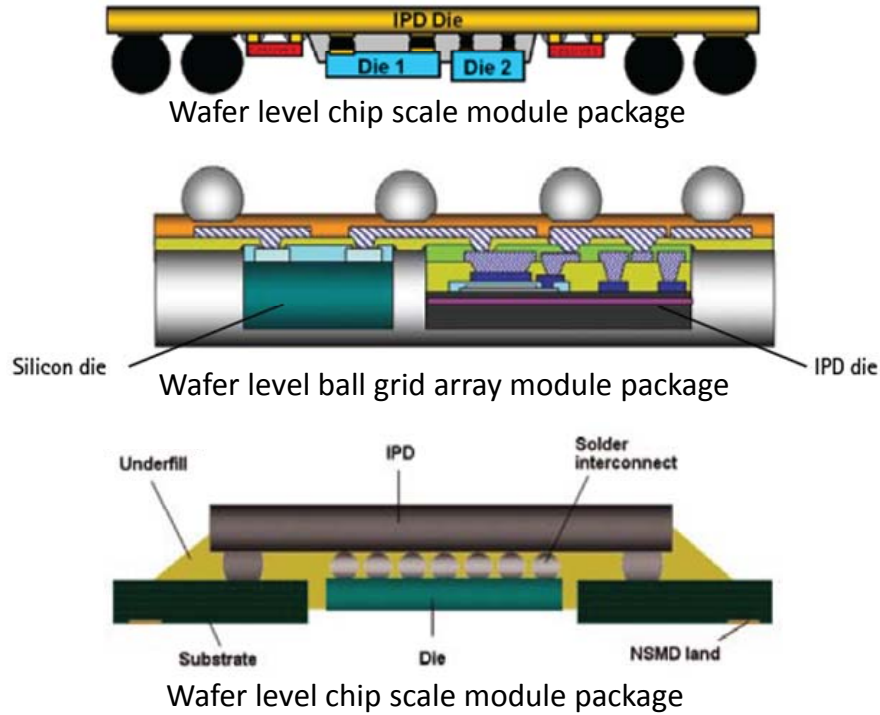


Figure 62: examples of module packages types incorporating IPDs

EMBEDDED ACTIVE DEVICES

Today’s consumer products place a premium on thin products and thin components. One of the primary driving forces for embedded active devices is to reduce total package height. Common applications with market history and forecast for embedded active devices from GSA Forum V21 No.1 are shown in figure 63.

Product	2012	2013	2014	2015	2016	2017
Power management modules	0.5	7	10	15	75	90
Power modules (voltage regulators)	110	120	180	240	280	300
Automotive	0.005	0.2	40	57	60	70
FO-WLP *	616	702	869	1,043	1,276	1,517
RF modules/boards	1	2	10	60	130	220
Application processor for PoP (lamine process)	-	-	80	185	213	245
Medical (hearing aids)	-	-	0.45	2.66	2.7	2.8
Total	727.5	831.2	1,189.5	1,602.7	2,036.7	2,444.8

Source: TechSearch International, Inc.

Figure 63: Market forecast in millions of units/year for embedded active devices

Fan out WLP incorporates baseband, RF and power management ICs

Representative package types for embedded actives are shown in Figure 64 below. A large number of variations of embedded active package architecture can be generated to fit the application limited only by stress and thermal management constraints. New materials and processes will reduce both of these problems significantly due to lower temperature process and new materials for thermal management and reduced CTE differential under development today are available.

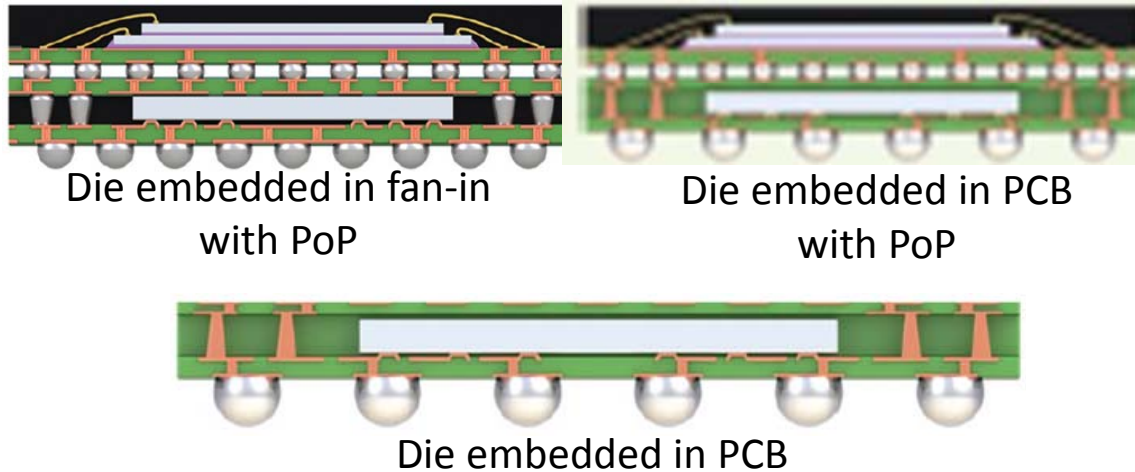


Figure 64: Examples of Active die embedding architectures

WAFER THINNING AND SINGULATION

Wafer thinning and singulation processes are well known and equipment for these processes is available. The technology today can produce wafer with the thickness required through the 2030. The minimum wafer thickness is shown in Table HI-27.

A few challenges remain that must be addressed and they are presented in Table HI-28. The most critical issue, thinning wafer/die for stacking, is a cost effective process for the removal of adhesive residue after the thinning process. There are multiple 2-step processes available for adhesive residue removal after the thinned wafer is released but they add to cost. The most desirable solution would be an adhesive that can be easily removed with zero residue. Despite significant effort this material is not yet available.

Wafer thinning and singulation process flows for single die, heterogeneous die on wafer and stacked wafers are shown below in Figures 65, 66 and 67 respectively,

Single Die Flows

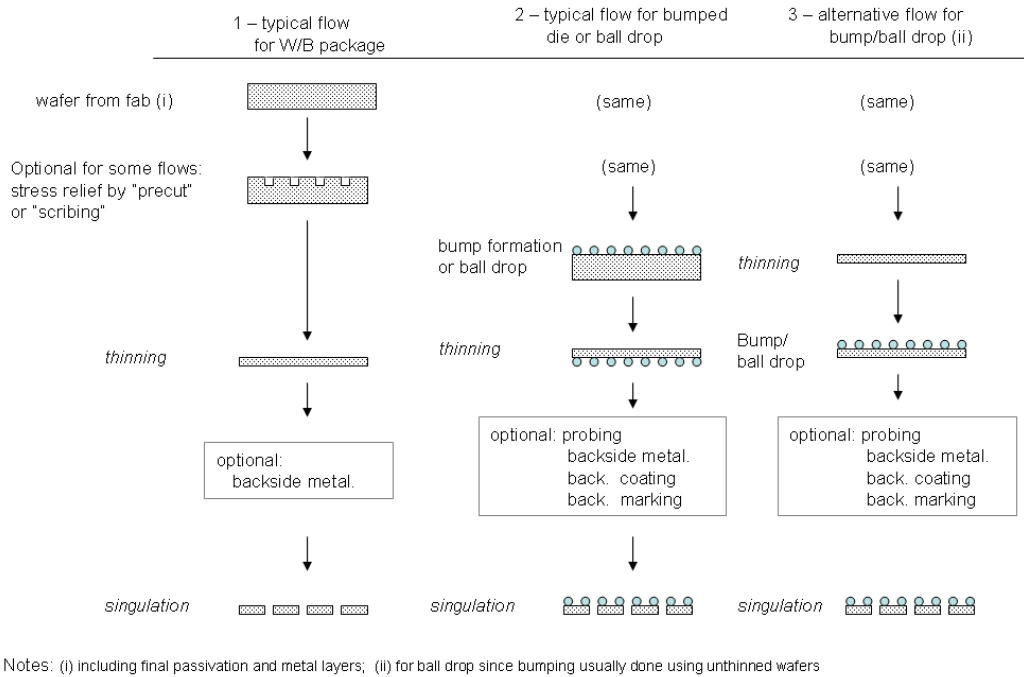
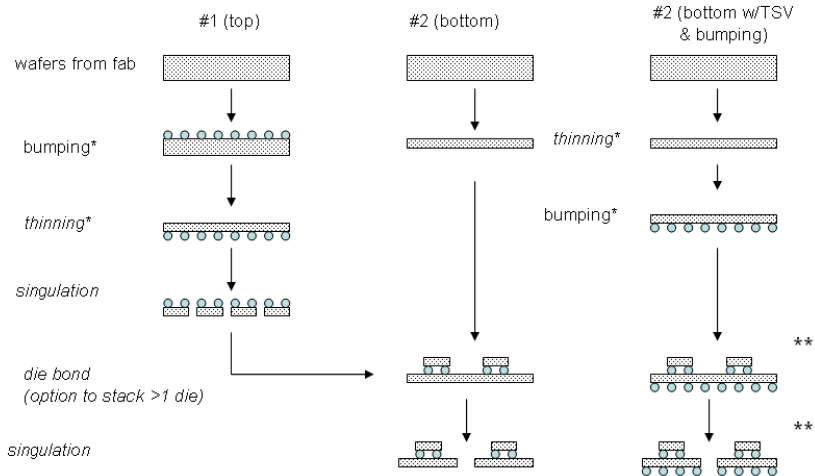


Figure 65: Extract of Thinning & Singulation Process Flow for Single Die Package

Heterogeneous Stacked Die / Die-on-Wafer (based on 2-die case, stack additional die as needed**)



* may change order of bumping & thinning

**presents handling challenge

Figure 66: Extract of Thinning & Singulation Process Flow for Packages using Die on Wafer Process

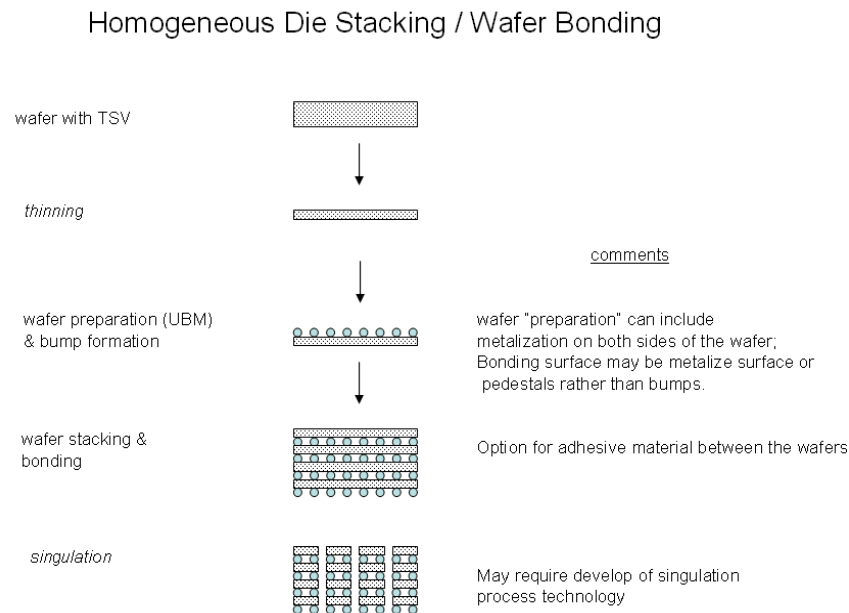


Figure 67: Extract of Thinning & Singulation Process Flow for Packages using Bonded Wafers

12. PACKAGING MATERIALS REQUIREMENTS

SCOPE

The incredible progress over the last 45 years was predicted by Moore's Law and followed predictable paths of shrinking geometries, improving designs and expanding wafer size. The devices to be packaged changed in area, thermal density and operating frequency but these changes were anticipated more than a decade in advance of the need thanks to the ITRS.

The materials used for packaging logic and memory semiconductor electronics changed slowly for many years and the changes were more incremental than revolutionary. Today packaging materials contribute significantly to the packaged device performance, reliability, and workability as well as to the total cost of the package.

In the first decade of the 21st Century this changed dramatically. "More Moore" and the advent of "More than Moore" initiatives, the challenges for packaging have expanded from requirements for traditional packaging of future generations of logic and memory devices to include new component types such as Micro Electro Mechanical Systems (MEMS), radio frequency devices, power devices, photonics, plasmonics, other devices and several replacements for the CMOS switch as logic, high speed memory and high

density slow memory all have different solutions. Many of these devices involve heterogeneous integration of diverse materials and diverse circuit types bringing new packaging challenges related to differences in thermal, optical and mechanical properties.

These new device types, the failure of packaging cost to scale with time, changing environmental controls, the limitations of traditional packaging solutions to adequately address the rapid expansion of power density and bandwidth requirements as well as the coming end of CMOS scaling have demanded innovation in packaging. New processes have been developed such as wafer thinning, wafer level packaging, die attach films, copper pillars, copper wire bonds, embedded active and passive components, as well as 2.5 D and 3D integration. During the 2000-2015-time period these innovations resulted in a 100% change in the packaging materials for the most advanced packages. Examples of these changes are presented in Figure 68 below:

Function	Material in 2000	Material Today
Solder	High lead content solders	Lead free solders
Chip to package interconnect	Gold wire bonds	Copper wire bonds
Inter layer Dielectrics	Silicon dioxide, polymers	CVD ultra low κ dielectric
Package substrates	Laminate containing Halogen	Halogen free laminates
Die attach	Liquid epoxy	Epoxy film
Mold compounds	Filled epoxy	Higher filler modified epoxy
Thermal interface materials	Filled silicones	TBD
Under fill	Filled liquid epoxy	Blended filler epoxy
Adhesives	Acrylates	Epoxy
Nano-materials	Not used	Not used
Substrates	Epoxy E-glass	Filled BT/epoxy E-glass and S-glass
BU Substrate	BU Layer: solder mask Core: standard substrate	BU-Layer: Ajinomoto films Core: low CTE substrate

Figure 68: Changes in packaging materials occurred from the year 2000 to 2015

Most of these materials will change again during the 15-year time frame of this Roadmap. Some of these changes are in the later stage of development today and will move into production over the next 2-3 years. These include nano-solders, improved conductors and new dielectrics that include both ultra-low κ and high κ dielectric films to address capacitance needs of both the interconnects of the die and the package and provide small, high value capacitors for decoupling inductance and filtering noise at its source.

The Emerging Research Material Chapter will address the materials requirements for packaging with material developed jointly between Heterogeneous Integration and

Emerging Research Materials. The ERM horizon is 25 years and it may take that long for some of the composites incorporating ballistic conductors will be ready for production use. We incorporate their work by reference here.

The packaging challenges over the 15 years covered by this edition of the roadmap will demand even greater innovation in packaging materials. These materials properties must meet a widening array of required properties illustrated in Figure 69. This “6-axis optimization” of properties is the key to meeting performance and reliability requirements. Even when this is accomplished the low cost requirements may prevent adoption of promising new materials.

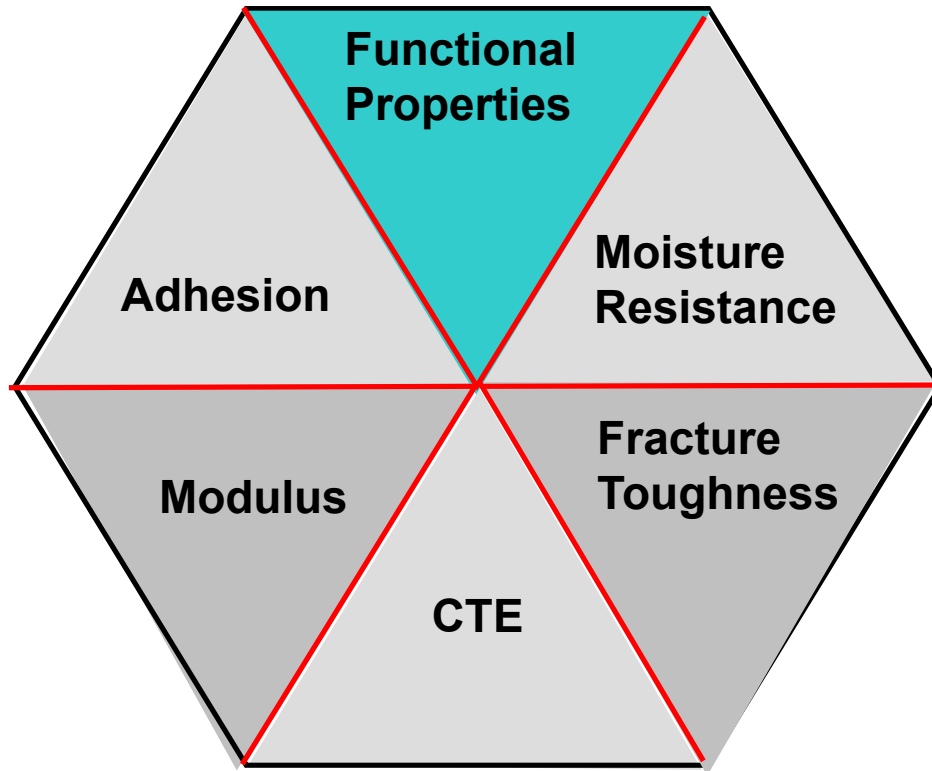


Figure 69: The materials properties requirements for packaging materials are highly coupled.

New materials will be required to achieve optimal properties for packaging applications in order to deliver device performance, reliability and low cost.

The organization of this section will be by class of material and, where possible, we will forecast the insertion points for new materials in the tables. The classes of materials are dielectrics, polymers, conductors, ceramics, nano-materials, composite materials and barrier layers. Polymers are often used as dielectrics but will be treated as a separate category due to their unique characteristics and diverse applications. A more detailed treatment of the packaging materials challenges and potential solutions can be found in the Emerging Research Materials Chapter.

DIELECTRIC MATERIALS

In traditional on-chip packaging the dielectrics are primarily polymers such as epoxy or polyimide. As the package substrate geometries shrink and both performance and power efficiency must increase, dielectric properties not available in polymers will be needed. The classes of dielectrics and their potential applications are listed below.

Material	Key properties	Applications
Solid and porous polymers	Low cost, spin-on, photoimageable, mechanical flexibility, low temp processing	Substrate wiring insulators, WLP, 3D assembly
Low κ dielectrics	Dielectric constant <3.0, high breakdown field strength, low leakage, low dielectric loss	2.5D, silicon package substrates, possible wafer level packaging
High κ dielectrics	Dielectric constant >10, high breakdown field, low leakage, low dielectric loss	Decoupling capacitors and filters for package substrates, 3D, 2.5D in wiring layers

Figure 70: Key properties of dielectric materials and their applications

SOLID AND POROUS POLYMERS

Although polymers have been used as inter layer dielectrics in packaging for decades, new polymers and polymer based composite materials will be required in the future. Properties required include:

- Lower dielectric constant
- Improved interfacial adhesion
- Lower coefficient of thermal expansion
- Reduced loss tangent at >1GHz
- Stable properties with humidity changes
- Lower processing temperature
- Improved resolution in photo-imaging
- Compatibility with higher temperatures in higher level assembly processes and harsh environments
- Higher thermal conductivity

LOW κ AND ULTRA-LOW κ DIELECTRICS

Traditional packaging has not required low κ dielectrics since the geometries were large, total wiring length was short and power efficiency of the package was not critical. In the semiconductor electronics roadmap reduced power consumption is essential and reduced capacitance in the device and packaging interconnect is part of the solution. As package substrate geometries shrink, operating voltage decreases and frequencies increase, the properties of traditional polymer dielectrics will no longer meet all the requirements.

Although low k dielectrics are not essential today, in the future they will be needed for 2.5D packaging, 3D packaging and WLP. There are three materials that are candidates to meet these requirements; fluorinated polymers, porous polymers, porous CVD and porous spin-on dielectrics. Each of these has advantages and disadvantages for specific applications but none have yet demonstrated ideal characteristics for any of the applications.

HIGH K DIELECTRICS

The reduction of power and ensuring reliability as we shrink geometries is best addressed by a reduction of the operating voltage. Reliable operation requires maintaining the voltage within a narrow range as we approach the sub-voltage threshold for the contents of the package. Similarly, at lower operating voltage the electrical noise levels must be reduced to maintain an adequate signal to noise ratio. Both of these requirements can be satisfied by placing capacitors close to the transistors to decouple inductance for power delivery and filter noise. The use of high k dielectrics between local power and ground areas is the logical solution. Today the typical dielectric used has $\kappa \sim 4$. The ideal material should have $\kappa > 50$ with breakdown field strength $> 10E6v/cm$ and leakage currents $< 1E-9/cm^2$ at $1E6v/cm$. High k polymers filled with higher k dielectrics e.g $BaTiO_3$ is a solution for some applications. Today these materials do not satisfy all properties required (such as very thin layers for example) but promising work based on glasses formed from complex metal oxides is underway.

POLYMERS

Polymers have been the base materials of choice for package dielectrics, package encapsulation, under fill, adhesives and thermal interface materials since the co-fired multi-layer ceramic package was replaced by plastic body packages for high performance devices. Today polymers dominate these package components but they are very different from the first polymer materials used for these applications. In addition, polymers are candidates for optical waveguides and interposer materials for 2.5D and 3D packages. A wide range of polymers is used for these applications but they fall short of the properties that will be needed in the future. The reactive groups in packaging chemistries have experienced little change: acrylates are used in photoresists, arylate/epoxy blends are used in solder masks, BT/epoxy blends in dielectrics and epoxies in mold compounds, die attach and underfill materials.

DIE AND OTHER COMPONENT ATTACH MATERIALS

Die attach has become more complex due to die technology changes such as:

- Thin die (50 microns, and less) that are highly flexible
- High thermal dissipation requirements
 - Thin die attach adhesive layers with high thermal conductivity
 - Minimal voiding
- Air bridges on die making placing die without damage more difficult
- Fillet control (fillets around all sides but not up the side to the active surface)
- Location tolerance control of +/- 5 microns in X, Y and Z and below.
- Adhesion to a variety of interfaces (Glass, polymer, metal, oxides, etc.)

A variety of materials have been developed and more are in development to address these needs. In addition to new organic based compounds, usually filled epoxies, a variety of die attach films have been introduced.

Die attach films are applied to wafers before singulation so that die have an adhesive layer on them after singulation. These die are placed on a substrate that is preheated and immediately cure to at least a b-stage locking the die in place. A variety of these films are available with various properties: high thermal conductivity, high electrical conductivity, a variety of thickness and moduli.

The typical polymers used today for key applications and the key properties for each application are listed in Figure 71 below.

Application	Today's Material	Key parameters
Package body (molding compound)	Epoxy	Mechanical strength, low temperature processing, moisture barrier, shrinkage, low CTE
Encapsulant (wire bond, glob top)	Epoxy	Mechanical strength, low temperature processing, moisture barrier, shrinkage, low CTE
Dielectric (interconnect insulation)	Various	Photoimageable, low κ , low processing temperature, low CTE, Low loss tangent
Underfill	Various	Low shrinkage, low viscosity before cure, low temperature processing, high thermal conductivity, low CTE, interfacial adhesion,
Adhesives		Both conducting and insulating versions, low cure temperature
Thermal interface materials	Filled polymer	High thermal conductivity, low CTE, low processing temperature
Temporary bonding for thinned wafers/die	Thermal release polymer	Low cost, low temperature processing, zero residue, chemical compatibility with BEOL processes
Optical Waveguides	Not yet used	Low loss, CTE match to substrate, process compatibility with BEOL processing, low cost
Substrates		Low CTE, low Dk/Df

Figure 71: Key properties of polymers for typical packaging applications

Virtually all polymer layers exhibit some “bleeding” and this will become more limiting as the packaging geometries continue to shrink. The use of photoresist has not been addressed since it does not typically stay in the package. It should be noted that it is used

in packaging and in addition to its resolution and process resistance improved outgassing properties are needed to avoid contamination of bonding surfaces.

CONDUCTORS

Conductors have been used in packages for wiring, contacts, joining, interconnection, heat sinks, shielding and physical protection of the package contents. The conductors were metal and the materials of choice were typically copper, aluminum and gold. Emerging package types with TSVs have also used tungsten. New composite materials are beginning to be used in specific applications such as conducting adhesives and new classes of conducting materials will be used to meet future requirements. The nano-material conductors such as nanotubes, nano-wires and graphene will be addressed in the nano-materials section.

The metallic conductors present challenges that are increasing with shrinking geometries and higher current densities. These include:

- TCE mismatch with semiconductors and package substrates
- Electromigration
- Conductivity decrease due to grain boundary and edge scattering and decreased wire diameter
- Lack of mechanical strength
- Limited thermal and electrical conductivity (relative to future requirements)
- Intermetallic growth
- Surface finish/surface protective layers
- Bondability (solder, thermal compression bonding, direct interconnect bonding (DIB), etc.)
- Chemical properties (corrosion)

Solutions to some of these challenges are being met by multi-layer interfaces for contact pads and selecting “compromise” metals to meet a requirement such as tungsten for TSV fill to reduce CTE mismatch with the silicon. There is promising work underway on composite metal structures incorporating nano-materials to improve thermal, mechanical and electrical properties while maintaining compatibility with existing processes and equipment. These materials will be addressed in the composite materials section that follows.

CERAMICS

Ceramic packages became the dominant packaging solution for microprocessors and other high power, high performance and high reliability devices following the development of low temperature co-fired ceramic (LTCC) packaging. This technology is

still used for certain high value/high performance class packages but there is no major change projected for this technology in the future particularly for thermal conductivity advantages. The applications for this technology today are for harsh environments such as medical, power, communications space and automotive under the hood requirements. The emerging requirement for interposers for 2.5D and 3D is a potential future use for ceramics which is under investigation.

NANO-MATERIALS

Nano-materials have properties that satisfy many of the difficult challenges for semiconductor packaging. The list of leading properties is long and work is underway to incorporate these materials into device manufacturing as well as packaging. They include:

- Superior barrier properties
- Superior electrical conductivity
- Superior thermal conductivity
- Potential to be largely transparent
- Superior mechanical strength
- Superior processing properties (inks/solders/other)

Examples of these nano-materials with their key properties and potential applications in packaging are listed in table shown in Figure 72.

Material	Properties	Applications
Carbon nanotubes (CNT)	Mechanical strength, thermal conductivity, electrical conductivity	Transparent conducting films, conductors, composite materials, EMI shielding
Graphene	Barrier properties, electrical conductivity, thermal conductivity, mechanical strength, transparent to visible light	Transparent conducting films, barrier layers, heat spreaders, EMI shielding
Nano wires	Electrical conductivity subject to edge scattering, mechanical strength	Transparent conducting films,
Nano particles	Thermal conductivity, high κ , electrical conductivity	Filler to improve thermal properties, filler for conductive adhesive, low sintering temperature, low temp Pb free solder.

Figure 72: Nano-materials and their key properties for typical applications

Despite these proven properties these nano-materials have yet to penetrate the supply chain in any significant volume for either packaging or devices. These materials all have challenges that must be resolved before they can be incorporated for use in electronic packages. For example, graphene has wonderful barrier and mechanical strength but it is not available in large area format. CNT has the best thermal and electrical conductivity but cannot make an ohmic contact on both ends. Nano wires are not yet well characterized but they are subject to edge scattering and dangling bonds on the surface that limit the usefulness of their favorable properties. Nanoparticle dynamics are complex

and not yet well understood. The exceptionally high surface to volume ratio of nanoparticles enables soldering at below 200°C with pure copper.

COMPOSITE MATERIALS

Naturally occurring materials do not meet many of the future materials requirements for packaging and even such new materials alone fail to meet the “6-axis optimization” required. Composite materials consisting of filled epoxy and other polymers have been used for some time in packaging to enhance mechanical, electrical and thermal properties. The range of these composite materials will continue to expand with incorporation of new polymers and new filler materials to continuously improve the performance and reduce the cost. The use of nano-materials as fillers will expand the range of application for composite materials. Examples include:

- Improved thermal and electrical conductivity of copper while also increasing the mechanical strength. (Cu and CNTs)
- Improved EMI shielding while reducing the size and weight of packaging (CNT and graphene)
- Improved Transparent conducting films (graphene and CNT; graphene and silver nanowires)
- Improved inks for printed electronics (CNT, CNT and graphene)
- Improved thermal and mechanical properties of under fill and die attach
- Improved thermal and mechanical properties for molding compounds
- Improved thermal properties for thermal interface material
- Improved processability e.g. lower temperature solders and die attach, controlled viscosity and flow in underfills

The key challenge for incorporating nano-materials into composite materials is the dispersal and functionalization of the nano-materials. The work is still in its early phases. Many early attempts to improve thermal, mechanical and electrical properties with CNTs have fallen short of expectations due to inadequate functionalization of the CNTs to ensure proper dispersal and proper interface with the base material.

BARRIER LAYERS

In the past there have been specialized barrier layers developed such as isolation in a TSV structure for example. Barrier layers are required in many packaging applications to prevent liquid and gas contaminants from entering a package and to isolate sections of a package from other components. These requirements will increase as more complex SiP packages and MEMS structures incorporating microfluidics in either discrete packages or as SiP components are introduced. The barrier properties of graphene are superior to any other known material and potentially change the size and weight of advanced packages and potentially eliminate any need for separate EMI shielding.

13. RELIABILITY

PACKAGING RELIABILITY

SCOPE

The section will cover reliability issues related to packaging at a high level, while several other preceding sections cover reliability on specific packaging types. Packaging reliability is dependent on component design, construction, materials, processes and end use conditions. As new packaging technologies emerge, interactions need to be investigated for complex multi-component packages, stacked die packages, wafer level packages, thinned die packaging, SiP, 3D integration, MEMS, and heterogeneous integration. Advanced packaging technologies with new materials and assembly processes are exposed to additional causes of failure that are not yet fully characterized, or known at this time. Failure mechanisms for advanced packaging and potential solutions are also described in this section.

PHYSICS OF RELIABILITY

Reliability is the probability that a manufactured item will perform its function for the intended service life under the system operating and environmental use conditions. Packaging reliability is dependent on component design, construction, materials, processes and end use conditions. Advances in packaging technologies, materials and manufacturing processes require knowledge and application of the physics of failure mechanisms to ensure long term reliability. The application use conditions must also be well characterized and understood to drive a physics of failure based approach. Stress mechanisms that can negatively impact reliability include electrical, mechanical, thermal, chemical and environmental.

Modeling and simulation at the design stage for advanced packaging technologies and materials are required to identify weaknesses, assess risks and establish design rules for the following:

- Electrical signal and power integrity associated with higher frequency/current and lower voltage switching, electromigration at high current density, EMI, and power disruptions.
- Mechanical stresses due to shrinking interconnect geometries, low stand-off interconnects, CTE mismatch, warpage, and material properties.
- Thermal stresses due to increasing power density and dissipation with lower junction temperature designs.
- Use condition and environmental exposures such as temperature, humidity, corrosive environments, vibration, and drop/shock resistance.

COMPONENT INTERACTION RELIABILITY ISSUES

Packaging provides electrical, mechanical, thermal and environmental protection to semiconductor devices. Unknown interactions in new technologies and materials need to be investigated for complex multi-component packages, stacked die packages, wafer level packages, thinned die packaging, SiP, 3D integration, MEMS and heterogeneous integration of different circuit fabrics (memory, logic, analog, photonic, and different semiconductor materials). Potential interactions that can impact reliability include the following:

- Chip to substrate interactions for finer pitch copper wire bonding, new wire bond materials, die attach films, molding compounds, ultra low κ dielectric damage, flip chip metallization, copper columns, Pb-free solder alloys, underfill materials, CTE mismatch, moisture resistance, substrate core thickness and material properties, and substrate build up layers, via stacking construction and material properties.
- Package to package (PoP) interactions for package warping, packaging materials, package stacking design and construction, chip stacking within the package, assembly process parameters, solder joint integrity, underfill material properties, thermal gradients, and heat dissipation.
- Package to PCB interactions for substrate pad and PCB plating, Pb-free solder alloy, soldering issues, warpage, CTE mismatch, solder fatigue, mechanical bending and strain, vibration, shock, maximum operating temperature for long term reliability, and system level reliability requirements in the application use conditions.

FAILURE MECHANISMS

In addition to well-known failure mechanisms, advanced packaging technologies with new materials and assembly processes are exposed to additional causes of failure that are not yet fully characterized, or known at this time. Packaging failure mechanisms primarily initiate due to thermal and mechanical stresses, but may also be caused by electrical stress and chemical exposure. Potential failure mechanisms for advanced packaging include the following:

- Chip cracking due to thermal and mechanical stresses.
- Interfacial delamination or cohesive fracture of ultra low κ interlevel dielectric, new adhesives, die-attach materials and underfills.
- Interfacial cracking and deformation of metallization layers.
- Copper column stresses on the chip interconnect.
- Pb-free flip chip solder fatigue.
- Stacked chip adhesive failure, and interconnect fatigue.
- TSV voiding in filler material and sidewall isolation integrity for high aspect ratio TSVs.
- TSV interconnect metal fatigue or cracking, and die cracking due to differential thermal expansion (CTE mismatch).

- Electrical leakage and shorting due to loss of dielectric integrity between TSVs.
- Fracture of embedded active and passive components.
- Organic substrate interconnects failure.
- Electromigration failure.
- Contamination, corrosion and metal migration.
- Thermal oxidations of interconnect interfaces.
- Diffusion, void formation, and excessive intermetallic formation.
- Fine pitch lifted copper wire bonds, chip pad cratering, and corrosion due to molding compounds.
- Moisture outgassing induced cracking.
- Assembly defects.
- Warpage due to thermal gradients in stacked packages.
- Mechanical bending, vibration and drop/shock interconnect failure.
- Thermal cooling solution induced damage.

POTENTIAL SOLUTIONS

In many cases, failure detection and isolation will be challenging for advanced packaging technologies. Improvements in reliability can be designed into semiconductor devices by redundancy, and continuous test in operation with dynamic self-repair. Built in self-test (BIST) capability can facilitate identifying the cause of failure. Adequate margin must also be employed to minimize risk in the application conditions.

Enhanced accelerated life testing methods will also need to be developed to identify new failure mechanisms and weaknesses in the packaging design, construction and materials. Industry standard qualification tests are not adequate to identify new failure mechanisms in advanced packaging. Standard baseline acceptance tests for use in qualifying electronic components are targeted to accelerate known semiconductor device and packaging failure mechanisms, and do not correlate to application use conditions. For advanced packaging, reliability testing to failure is required to characterize the failure mechanism and develop acceleration models for use conditions. It is recommended that new failures mechanisms be addressed by building an understanding of the mechanism by means of accelerated stress conditions. Historically prescribed stress tests that do not correlate to the actual use environment may not accelerate valid failure mechanisms of concern.

Accelerated reliability test conditions and durations need to be customized based on the component under test, and match the range of end user application conditions (potential failure mechanisms, environment, and life time requirements). Typical stress test methods and conditions include temperature cycling, power cycling, temperature, humidity, voltage, electromigration, vibration, mechanical drop/shock and bend testing. A well designed test vehicle representative of the chip interconnect, packaging

construction, materials and assembly processes is often required. Functional devices may not have adequate electrical test sensitivity for interconnect failure detection and isolate. Electrical in-situ monitoring during packaging reliability stress testing is recommended to detect transient failures that can be missed at room temperature testing. Test vehicles can also aid failure analysis to identify the location and cause of failure.

Product life can be predicted based on failure mechanisms of concern, and correlating accelerated test results to product use conditions. The reliability prediction must be based on the design life of the product and the application use conditions. Some well known reliability prediction models include the Arrhenius model for thermal effects, Eyring model for temperature and voltage, Peck's Model for temperature and humidity, and Coffin-Manson and damage accumulation models for solder fatigue. Reliability predictions for advanced packaging require validation of existing models and development of models for new failure mechanisms.

CONCLUSION

Ensuring reliability in advanced packaging is a significant challenge. A great deal can be done to identify nascent defects, develop continuous test methods in operation with dynamic self-repair, intelligent use of redundancy, and graceful degradation. Advances in packaging technologies, materials and manufacturing processes require knowledge and application of the physics of failure mechanisms to ensure long term reliability. Interactions in new packaging technologies and materials need to be investigated to identify and characterize new failure mechanisms. Modeling and simulation at the design stage for advanced packaging technologies and materials are required to identify weaknesses, assess risks and establish design rules. Enhanced accelerated life testing methods will also need to be developed to identify new failure mechanisms in advanced packaging design, construction and materials. Reliability testing to failure with in-situ monitoring using test vehicles representative of the chip interconnect, packaging construction, materials, and assembly processes are required to characterize failure mechanisms and develop acceleration models for end use conditions and environments.

REFERENCES

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- JEP132 Process Characterization Guideline
- JEP156 Chip-Package Interaction Understanding, Identification and Evaluation
- JEP158 3D Chip Stack with Through-Silicon Vias (TSVs): Identifying, Evaluating and Understanding Reliability Interactions
- JEP122 Failure Mechanisms and Models for Semiconductor Devices
- JEP148 Reliability Qualification of Semiconductor Devices Based on Physics of Failure and Risk and Opportunity Assessment
- JEP150 Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components

- JESD47 Stress-Test-Driven Qualification of Integrated Circuits
- JESD91 Method for Developing Acceleration Models for Electronic Component Failure Mechanisms
- JESD94 Application Specific Qualification Using Knowledge Based Test Methodology

14. PACKAGING GAPS AND TECHNOLOGY NEEDS

The pace of change demands addressing a continuous flow of unmet technology needs that result in “gaps” in our capability that must be addressed. In a joint effort with INEMI we have initiated an activity to identify these gaps and update the list annually. The summary of this work is presented in Table HI-30. The table is arranged with a near term horizon of 5 years and a longer-term section. The objective is to focus the investment of the industry on these areas to close the gaps before they impact the pace of progress.

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